Electrical Engineering 234

Electrical Engineering Circuit Laboratory

Experiments

and

Laboratory Manual

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Contents

This manual and the experiments were compiled, written and/or edited by Robert C. Maher, Assistant Professor, with graduate assistant Duane T. Hickenbottom during Spring Semester 1992.

Laboratory Procedures and Reports

The purposes of this laboratory course are to practice essential laboratory measurement and report preparation skills, to reinforce the concepts and circuit analysis techniques taught in EEngr 214 and EEngr 260, and to gain an increased understanding of some of the practical issues of electrical engineering circuit analysis and design.

Lab Manual Format

Each of the entries in this lab manual consists of several sections: Abstract, Introduction and Theory, References, Pre-lab Preparation, Experiment, and Results.

The *Abstract* is a brief summary describing the experiment.

The *Introduction* and *References* sections provide some of the background information necessary for the experiment. This material is intended only to be supplementary to the classroom lectures and exercises in EEngr 214 and 260.

The *Equipment* section lists the major components and measurement instruments needed to perform the experiment.

The *Pre-lab Preparation* section contains several tasks that must be performed *BEFORE* arriving at the lab. The pre-lab typically requires calculation of specific component values, prediction of the behavior to be measured in the lab, and preparation using computer simulation.

The *Experiment* section contains a description of the circuits, components, and the actual lab measurements to be recorded in the lab notebook. This section is the *minimum* required effort: you are encouraged to try additional ideas once the required measurements are made. Ask the lab teaching assistant (TA) for guidance with this.

Finally, the *Results* section lists the **minimum** required items to be presented in the final lab report.

Lab Evaluation and Grading

Your grade in this laboratory course is based upon several components.

Pre-lab exercises	20%
TA evaluation of your lab skills and knowledge	20%
Lab practical final exam	20%
Lab results and reports	40%

The *pre-lab exercises* are to be turned in at the beginning of the lab period. If you need any of the pre-lab results in order to perform the experiment you will have to make a copy of your pre-lab solutions, preferably in your lab notebook. Your TA should grade the pre-labs during the lab period and return them to you before you leave.

The *TA evaluation of lab skills* will be based on how well you respond to the questions he or she will ask you during the experiments throughout the semester. In other words, the TA will occasionally ask questions to ascertain whether you (i) understand the theory and rationale for the experiment, (ii) are able to operate the lab instruments properly, and (iii) can express your knowledge in a meaningful, concise manner. *Hint:* if you do not understand the lab concepts it is probably advisable to ask your TA for help *before* he or she puts you on the spot!

A *lab practical exam* will be given in order for you to demonstrate your analytical ability and proficiency with the equipment, circuits, and concepts considered in this course. The content, format and schedule of the practical exam will be determined by your TA.

Finally, the largest individual component of your lab grade will be based on your *lab results and reports*. Some suggestions for your lab notebook and lab reports are given next.

Lab Notebook

Good laboratory practice begins with pre-lab preparation. It is essential to read the lab manual, perform the pre-lab assignments, and carefully think through all the steps to be performed and the measurements to be made. This process centers around the need for good documentation: a lab notebook.

The lab notebook is a complete record of ALL work pertaining to the experiment. It is not necessary to include lengthy explanations and procedures in the notebook, but *the*

entries must be sufficient for another person to understand your methods and replicate the experiment. The purpose of the notebook is to follow the required practices of industrial or academic research and development laboratories, where complete and accurate records of laboratory work are vital. The lab notebook is a legally recognized paper that is essential in documenting inventions, discoveries, and patent disclosures. Some companies require lab notebooks to be officially notarized and filed so that any legal questions later on can refer directly to the original, unaltered notebook entries. Although a notary seal is not required for your lab notebooks in this course, be sure to keep the importance of good experimental note taking in mind.

The pages of the notebook must be bound (not loose leaf or spiral) and should be numbered consecutively. The notebook entries must be in ink, and no pages should be left blank between entries. Begin the entries for each experiment on a new page, giving the title of the experiment, your name, the name of your lab partner, and the date. In case some of the data or calculations written in the notebook turn out to be in error, *do not* tear out the page or completely obliterate the entries: a *single line* through the error is preferred. This way there is no question regarding the legitimacy and completeness of the notebook material. ***Furthermore, you will <u>not</u> be penalized in this course for having lined-out errors and corrections in your notebook.***

Pre-lab preparation results can be written in the notebook, along with an outline of the experiment to be performed, circuit sketches, and anticipated results. The expectations and predictions from the pre-lab work are extremely important in guiding the measurements actually made in the lab. For example, if we expect a linear relationship (y = m*x) between two circuit parameters and measure something completely different, we are in a position to double-check the circuit and the measurement techniques to discover whether the discrepancy is due to an incorrect circuit, limitations of the measurements, or faulty assumptions and predictions. Similarly, the ideal number and spacing of data points on a graph can guide the number and spacing of lab measurements. Always determine the level of accuracy of each measurement and include these limitations with the results.

The process of comparing expectations and results is best accomplished *during* the lab period: this way any questionable data can be verified and further measurements can be made. Along with tables of the measured data it is useful to sketch graphs of the measurements. This helps to spot trends or errors in the data. For the same reason it is also desirable at least to "work through" the required solutions to the Results section of the experiment *before* leaving the lab.

Lab Report

All jobs in electrical engineering require proficiency in technical writing. The written lab report is just one example. The report should be written specifically to meet the needs of the reader, meaning that the writing must be brief, interesting, and complete. It is good engineering practice when writing to always begin with a *summary* of each important conclusion, followed by the *results and reasoning* that led to that conclusion, and finally a *review* of what was stated. Keep in mind that the specific format and content requirements of the lab report may vary depending upon the preferences of the reader, in this case the lab TA.

In addition to the technical content of your report, you will also be graded on your use of the English language. Be certain that your spelling, punctuation, and grammar are correct.

The report should be assembled in some reasonable manner, such as:

- Cover Page showing the experiment title and number, date experiment was performed, date report was finished, and the name of the author and partner.

- Abstract giving a summary of the *complete* report. The abstract is normally written last, and should ordinarily be no more than 3 or 4 sentences.

- Introduction giving a 1 or 2 paragraph explanation of what the reader must know to understand the report. Basically, the introduction indicates whether *you* understood what the lab was all about!

- Procedure describing the steps used in the lab. This need only be sufficient to recreate the experiment in conjunction with the lab notebook, *not* a lengthy minute-by-minute account.

- Results and Discussion of the experiment, including the requested information from the lab manual, comparisons with pre-lab predictions, and *reasonable* explanations of any difficulties or surprising results. Tables of "raw" data should be left in the notebook, not in the report, except where necessary to support the discussion. *Do* include graphs of the results where appropriate. Include a discussion of the methods and circuits used in the experiment and indicate any extra measurements or investigations you made in addition to the steps in the lab manual. Indicate important observations *you* were able to make that other students might have missed.

- Conclusion giving the main items learned in the experiment.

Before finalizing the report to turn in, look over the entire report with a critical eye. Is the report complete and concise? Is the substance of the report good enough *that you would show it to a potential employer* as an example of the quality of work you do? Does it indicate that you know what you are doing? Are the sections labeled? Are the graphs labeled and *interpreted* (slopes, breakpoints, etc. identified)? Are the circuit diagrams accurate and labeled? Do you tend to use imprecise phrases and meaningless platitudes like "very large", "negligible", "this experiment demonstrates to the student...", "the results validate the theory", "the measurements are cruddy because ideal conditions do not exist", etc.?

Lab Safety

A few simple electrical laboratory safety guidelines apply:

1) There must always be at least three people in the lab at one time: one able to assist an injured person and one to go for help.

2) All electrical apparatus that connects to the AC power line must have a protective ground through a three-wire power cable, or be of approved double-insulated construction.

3) Always check and re-check circuit wiring before applying power. Always have a single switch or button that will immediately remove power from the circuit in case of trouble.

4) Always switch the circuit power off before changing components or connections. *It is tempting to become lazy and change connections in low-power circuits with the supply on, but this is asking for trouble in the form of unintentional short circuits and blown components, or serious damage and injury in the case of high power circuits*.

5) Always ask for directions or help if you are unsure of the correct measurement procedure or circuit connection. *Be honest with yourself*: if you don't understand what you are doing, seek assistance from the lab TA.

Some Final Words...

This lab course has been put together to benefit a specific customer: *you*. If you are having difficulty understanding the experiments and concepts because of the way in which the material is presented, let your lab TA know! You will notice that part of the results section for each experiment is a question asking how you would change the experiment to make it more understandable, more interesting, and more useful to you.

This lab course covers a wide range of topics. A few of the topics you will probably find easy to master, while most topics will seem complicated and perhaps even incomprehensible. *Do not expect simply to walk into the lab without preparation and get the experiment accomplished!* You will need to allow sufficient time *before* the lab period to look over the experiment, understand the concepts and procedures, and prepare the pre-lab assignments. A few extra minutes in preparation will make your experience in the lab much more enjoyable and meaningful. Getting into the habit right away of setting aside a specific period of time each week for lab preparation will be much easier than always trying to squeak it in the night before the experiment is to be done.

In writing a lab manual it is difficult to avoid the need for a certain amount of cookbook directions: "assemble the circuit of Figure x, connect wire A to point B, write down the voltage at point C, repeat until done". Unfortunately, it is possible that some of you may begin to feel that good engineering laboratory practice consists entirely of following tedious directions. I have found many students and even working engineers who are extremely queasy about having to analyze the cause of a malfunctioning device or having to design or modify an electronic system to meet a specific requirement. The whole process of engineering can seem overwhelming when you are out on the job and no "cookbook" is available for every project.

As you work on the experiments in this course, keep in mind that electrical engineering involves a generous mix of *theory, analytical skills, creativity, and practical experience*. Theory and analytical skills are what you are taught in the classroom. Creativity involves a good understanding of the strengths and limitations of electrical engineering components, concepts, and technology. But of all the design ingredients, *practical experience* is perhaps the most important element. This course and your other lab courses are intended to help you gain some of this practical experience. Take this opportunity to try out your own ideas. Ask questions of your TAs, professors, electronics technicians, and even other students. Learn from your own mistakes--and learn from the mistakes of others! Besides, this lab should also be fun!

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Resistors
(5% tolerance, carbon or carbon film, 1/4 watt)

Qty	Nominal Value
2	100Ω
2	220Ω
1	300Ω
2	680Ω
1	750Ω
4	1kΩ
2	2.2kΩ
2	5.6kΩ
2	6.8kΩ
2	10kΩ
2	12kΩ
2	22kΩ
2	33kΩ
1	47kΩ
1	68kΩ
2	100kΩ
2	220kΩ
2	430kΩ
2	470kΩ
2	1MΩ

Semiconductors

Qty	Component
1	Type 741 Op amp
1	Type BS170 NMOS Enhancement FET (not BS170P !)
2	Type 2N2222 NPN BJT
4	Type 1N4001 Silicon Diode

Capacitors

Qty	Nominal Value and Type
2	0.001µF (100 volts, polyester or plastic film, ±10% tolerance or better)
2	0.0022µF "
2	0.01µF "
2	0.022µF "
2	0.047µF "
2	0.1µF "
2	0.22µF "
2	10µF (35 volts or more, aluminum electrolytic, ±20% tolerance or better)
4	22µF "

Lab # 1
TITLE: Response of RLC Circuits

ABSTRACT

This experiment considers the response of simple series RLC circuits. It should be noted the solutions for parallel RLC circuits are duals of the solutions for series RLC (replace **R** with **1/R**, **L** with **C**, **i** with **v**) As with RC and RL circuits, the output of any RLC circuit can be analyzed to determine the total response, consisting of both the steady-state (forced) response and the transient (natural or complementary) response, for any given input. Our analysis will cover only constant (DC) forcing functions as inputs. This lab includes SPICE analysis and construction of simple **series** RLC circuits.

INTRODUCTION AND THEORY

Linear second order systems are common to many fields of study. Mechanical engineers use the same equations to solve for the displacement of a spring-supported mass subjected to viscous damping and physicists solve for the motion of a simple pendulum. While electrical engineers usually solve for the current or voltage in a circuit, mechanical engineers may solve for displacement or motion of a mass. No matter what physical components are used (inductors or springs, capacitors or masses, resistors or dashpots) or the response desired (current or force, voltage or velocity), the same form of solutions will be obtained (damped, overdamped, or critically damped). The same equations are also very important in control systems analysis (EEngr 444).

Many circuits used in communications networks can be modeled well by combining ideal resistors, capacitors, and inductors. RLC circuits are an important part of some of the electronic amplifiers found in every radio receiver and allow the amplifiers to produce a large voltage amplification over a narrow band of signal frequencies and nearly zero amplification outside this band. Parallel RLC circuits are also used in multiplexing filters and harmonic suppression filters.

Previous experiments with RL and RC circuits involved only one storage device and were solved with a first order differential equation. Circuits involving both inductors and capacitors require solving a 2nd order differential equation.

$$\frac{d^2 i}{dt^2} + \frac{R}{L}\frac{di}{dt} + \frac{i}{LC} = 0,$$

or

$$\left(s^2 + 2\alpha s + \omega_o\right) I = 0.$$

For the second form, α (exponential *damping coefficient*)=**R/2L** and ω_o (resonant frequency) = $(LC)^{-\frac{1}{2}}$. Often ω_o is normalized to 1 by substituting ζ (damping ratio)=$\boldsymbol{\alpha/\omega_o}$. Another important substitution (for the underdamped solution) is $\boldsymbol{\omega_n}$(natural or damped frequency)= $\sqrt{(\omega_o^2-\alpha^2)}$ The 3 most important forms of the solution for i are:

Case I: $\alpha>\omega_o>0$ ($\zeta > 1$) The *overdamped* case.
Case II: $\alpha<\omega_o$ ($0 < \zeta < 1$) The *underdamped* case.
Case III: $\alpha=\omega_o$ ($\zeta = 1$) The *critically damped* case

See the Irwin text for a comparison of the 3 cases. Notice the underdamped response reaches steady state fastest but overshoots. Overdamped does not overshoot but takes longer to reach steady state than the critically damped response. Critically damped reaches steady state as fast as possible **without** overshooting.

REFERENCES

See chapter 8 of the text by J. David Irwin, *Basic Engineering Circuit Analysis*, 4th ed., Macmillan Publishing Co., 1993 .

For help with PSPICE (esp. .STEP and .MODEL statements) see paperback by P. W. Tuinenga, *SPICE: A Guide to Circuit Simulation & Analysis Using PSpice®,* 2nd edition, Prentice Hall, 1992.

For electrical/mechanical equivalents, see section 2.7, by J.J. D'Azzo and C.H. Houpis, *Linear Control System Analysis and Design,* 2nd ed., McGraw-Hill Book Co, 1981, or the current EE 444 (Control Systems) textbook.

EQUIPMENT

Oscilloscope
Signal generator
Variable inductor (0.01 to 0.1 H by .01 H)
Assorted resistors and clips
Inductance/capacitance meter
0.1 μF capacitor
Potentiometer (0-1kΩ)
Ohmmeter

PRE-LAB PREPARATION

(I) Refer to Figure 1.1. For the pre-lab the voltage source is a 10 V power supply (with an internal impedance of 50 Ω) which is switched on at time t=0.

(a) Solve for i (current) through the potentiometer.
(b) What are α (damping coefficient), ζ (damping ratio), ω_o (resonant frequency), and ω_n (natural frequency)?
(c) Is the circuit over, under or critically damped? Why?

(II) Solve for $V_C(t)$, the capacitor voltage.

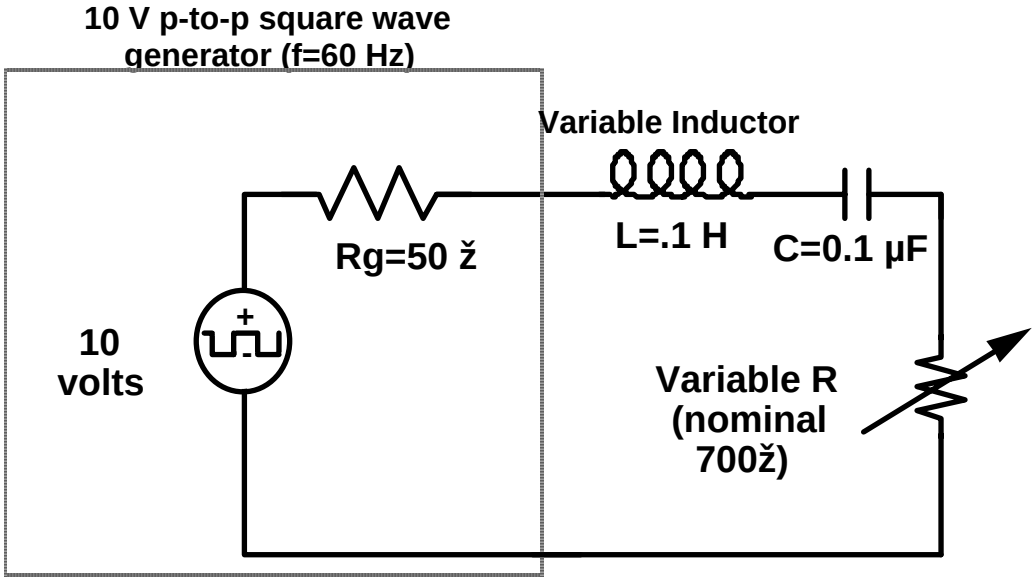

Figure 1.1

(III) Using the circuit of part (I), what value of resistance (R) will provide critical damping? What are α and ω_o?

(IV) Do a PSpice transient analysis using initial values from (I). Vary the **resistance** to get three plots showing under, over, and critical damping. Use PROBE to plot (a) the three currents and (b) $V_C(t)$, the three capacitor voltages, on two separate curves.

NOTE: First replace the 10 V step input with a 10 V peak-peak square wave which has a period long enough to show the underdamped response. (A square wave generator will be used in the lab to produce a periodic signal which can be viewed on the oscilloscope.) The three voltage or current curves may be plotted on the same curve either by creating three separate circuits driven by the same source, OR by using the `.STEP` statement. *For example*, a "stepped" resistor could be implemented using:

```
RSTEP 1 2 POTMOD 50K
.MODEL POTMOD RES
.STEP RES POTMOD(R) 0.95 1.05 0.05
```

On the first line of this example a resistor arbitrarily named `RSTEP` has a nominal value of 50K ohms and is connected between nodes 1 and 2 in the circuit. The resistor is described by a model arbitrarily named `POTMOD`. The second line is the model description for `POTMOD`, and states simply that this model is a resistor model (type `RES`). The last line of the example is the `.STEP` command which causes the entire PSpice analysis to be run for `RSTEP`=47.5K, 50K, and 52.5K, corresponding to the 50K nominal value and multipliers from 0.95 to 1.05 in 0.05 steps.

Measure the *overshoot* (%) and the *rise time* (t_r) where

$$\text{Overshoot (\%)} = \left(\frac{y(t)_{\text{maximum}} - y(\infty)}{y(\infty)} \right) \times 100\%$$

$$\text{Rise time } (t_r) = \text{time}\left[0.9 \cdot y(\infty)\right] - \text{time}\left[0.1 \cdot y(\infty)\right]$$

Rise time is defined as the time required for the response to move from 10% to 90% of the steady state value because it is difficult to measure exactly when the response reaches its final value. An example of rise time is shown in Figure 1.2.

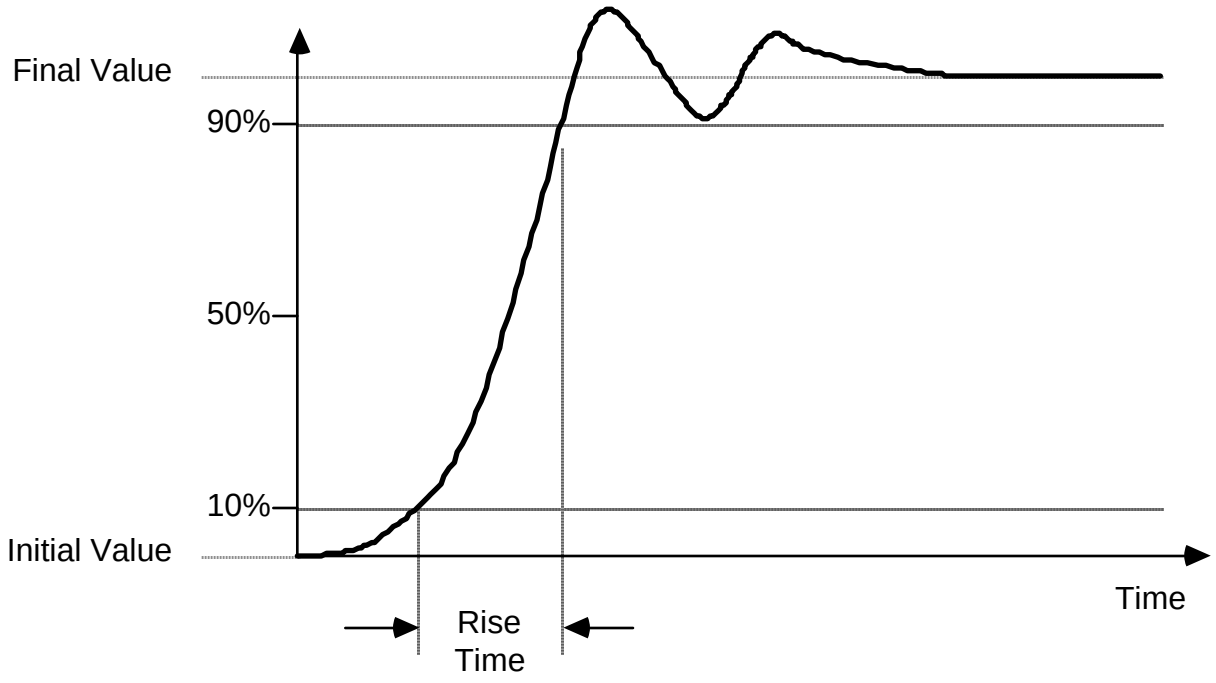

Figure 1.2

EXPERIMENT

(1) Use the inductance/capacitance meter to measure the inductance of the variable inductor for each setting. Use an ohmmeter to measure the internal resistance for each setting.

(2) Use the same meter to measure the capacitance and ESR (equivalent series resistance) of the capacitor.

(3) Connect the circuit as in Figure 1.1 but substitute a signal generator set to 10V (peak-peak) square wave for the 10V step input. Use a combination of resistors and a potentiometer to obtain the 3 values of resistance from prelab IV. NOTE: Use resistors from lab kit if you need to obtain resistance >1kΩ.

Measure and graph **i(t)** and $\mathbf{v_c(t)}$ for all 3 values of the resistance (from prelab IV).

Now adjust the potentiometer/resistors until critical damping is achieved (just before curve begins to overshoot). Measure the **actual** resistance needed to obtain critical damping.

(4) Adjust the resistance to the value (from prelab IV) which causes the circuit to be underdamped. By measuring the time period for one oscillation of the "ringing", determine ω_n (natural frequency).

RESULTS

(a) List the actual values of the inductor for each setting. Which setting had the largest % error? What was the % error in the capacitor value?

(b) Compare the SPICE i(t) and $v_c(t)$ curves to the lab experimental curves, especially the critically damped curve. Discuss the % overshoot, rise time, and the exact value of resistance for critical damping. What were the % differences and why?

(c) Using the value of ω_n determined experimentally (part 4), calculate the total resistance in this RLC circuit and compare to the value of R used in part 4. Discuss any differences.

(d) When viewing the square wave output of the signal generator (while connected to the RLC circuit), why is the square wave slightly distorted?

(e) Does the signal generator impedance affect the circuit performance? When might the generator impedance need to be taken into account? Does the internal resistances of the inductor, capacitor, and signal generator affect the response?

(f) Is there any part of this lab which you do not understand? What can be done to improve this experiment?

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Lab # 2
TITLE: Impedance I: Phasor Relationships for Simple Circuits

ABSTRACT

The response of an electrical network to a sinusoidal input forcing function is an extremely important characteristic in electrical engineering. This laboratory exercise investigates the amplitude and phase relationships between voltages and currents in electrical networks driven by sinusoidal sources. In particular, the concepts of *phasors* and *impedance* are examined.

INTRODUCTION AND THEORY

One of the first concepts considered in electrical engineering is the relationship between voltage and current in a resistor: v=iR (Ohm's Law). As we will see in this lab, it is also possible and useful to generalize Ohm's Law to represent arbitrary combinations of resistors, capacitors, and inductors, using the concepts of *phasors* and *impedance*. First, a description of the behavior of the basic circuit elements to sinusoidal input functions is considered.

Voltage and Current in R, L, and C

The meaning of Ohm's Law for resistors is unchanged if the voltage, V, and current, I, are allowed to be time-varying* . For example, if

$$v(t) = A \cdot \cos(\omega t + \phi),$$

then

$$i(t) = \frac{A}{R} \cdot \cos(\omega t + \phi),$$

where Ris the resistance in ohms,

- A is the amplitude of the time-varying voltage (volts),
- ω is the angular frequency of the signal (radians/sec),
- t is time (seconds), and
- ϕ is an arbitrary phase offset (radians).

* Note that although cosine "driving" functions are used here, sine functions apply just as well.

The important feature of this result is that the voltage and current are *in phase*, because the two waveforms have the same time dependence, $\cos(\omega t + \phi)$. It is true in general that the voltage and current in a resistor are *in phase*.

Now consider the relationship between current and voltage in an inductor: $v = L\, di/dt$. For example, letting the current be time varying,

$$i(t) = B \cdot \cos(\omega t + \phi),$$

then

$$v(t) = -\omega \cdot L \cdot B \cdot \sin(\omega t + \phi).$$

Using the relationships $\sin(\theta) = \cos(\theta - \pi/2)$, and $-\cos(\theta) = \cos(\theta + \pi)$, the expression for $v(t)$ can be rewritten

$$v(t) = \omega \cdot L \cdot B \cdot \cos(\omega t + \phi + \pi/2).$$

Note that unlike the resistor, the voltage and current for an inductor are *not* in phase. The total instantaneous phase of the voltage, $(\omega t + \phi + \pi/2)$, is always $\pi/2$ (one quarter cycle) greater than the phase of the current, $(\omega t + \phi)$. Thus, the *voltage leads the current* by $\pi/2$ in an inductor. In other words, the maxima, minima, zero-crossings, etc. of the voltage occur one quarter of a cycle before the corresponding extrema of the current.

A similar examination of the voltage and current relationship for a capacitor ($i = C\, dv/dt$) reveals that the *current leads the voltage* by $\pi/2$, i.e.,

$$v(t) = A \cdot \cos(\omega t + \phi),$$

then

$$i(t) = -\omega \cdot C \cdot A \cdot \sin(\omega t + \phi) = \omega \cdot C \cdot A \cdot \cos(\omega t + \phi + \pi/2).$$

Phasors

Although the voltage and current analysis of the basic circuit elements is relatively simple using trigonometric identities, the analysis situation becomes more difficult for networks involving combinations of the various elements. Consider for example the "simple" network shown in Figure 2.1.

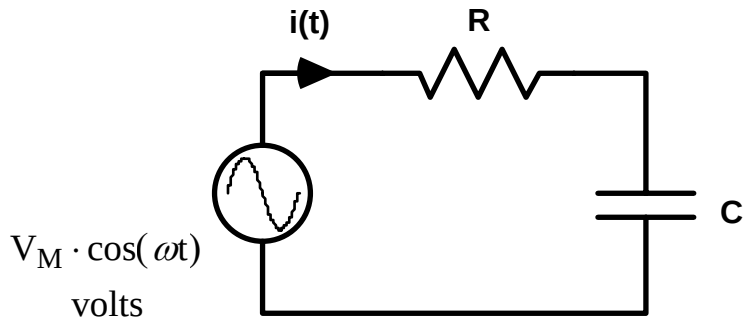


Figure 2.1

The conventional way to find the loop current i(t) is to solve the differential equation describing the circuit:

$$V_M \cdot \cos \omega t = R \cdot i(t) + \frac{1}{C}\int i(t)\ dt$$

.

Assuming the current is of the form $i(t) = \alpha \cdot \cos(\omega t + \varphi)$, we can determine the unknown constants α and φ, which gives the solution:

$$i(t) = \frac{\omega C V_M}{\sqrt{(\omega CR)^2 + 1}} \cdot \cos\left(\omega t + \tan^{-1}\frac{1}{\omega CR}\right)$$

or

$$= \frac{V_M}{\sqrt{R^2 + \left(1/\omega C\right)^2}} \cdot \cos\left(\omega t + \tan^{-1}\frac{1}{\omega CR}\right)$$

Solving the differential equation directly like this is certainly feasible for simple circuits, but this technique becomes rather unwieldy for circuits with more components, loops, and branches. The main difficulty is in keeping track of the phase relationships between the various nodes in the network. Instead, we will often use an analysis approach which makes use of complex number theory and the *linearity property* of the elementary circuit elements.

The complex number theory of interest here can be summarized by Euler's relationship

$$e^{j\omega t} = \cos \omega t + j\sin \omega t$$

Note that this allows us to convert between cosines and sines and a complex exponential form. The advantage to the complex exponential form is that we merely

need to *add* exponents when we multiply exponentials together. This will come in handy when the relative phase difference between voltage and current in a network is considered.

The concept of linearity that we will need is *superposition*. Recall superposition means that the total response of a circuit due to the sum of two or more inputs is simply the sum of the responses due to each input if acting alone. For our purposes here, *the usefulness of the linearity property is that we are free to introduce a complex exponential whenever it makes the mathematical analysis easier, as long as we remember to take the "real part" when we get to the solution*. In short, the imaginary part of the complex exponential simply "goes along for the ride" to assist with the mathematical analysis.

The other important result of linearity is that if the circuit is driven by a single sinusoidal (sine or cosine) source, *all the voltages and currents in the network will also be sinusoidal but with possibly different amplitudes and phases relative to the source*. In other words, each term in our network equations will contain the complex exponential factor $e^{j\omega t}$. This is the heart of steady-state sinusoidal analysis.

We will indicate the amplitude and phase relationship through the use of *complex notation*: a complex number is used to indicate only the *amplitude* and *phase* of voltages and currents in the circuit (since the sinusoidal time variation factor $e^{j\omega t}$ is common to all terms). For example, a circuit current described by the equation

$$i(t) = I_0 \cos(\omega t + \theta)$$

can be written in complex exponential form (Euler's equation) as

$$i(t) = \mathrm{Re}\left\{ I_0 e^{j(\omega t + \theta)} \right\},$$

and in polar complex form as

$$i(t) = \mathrm{Re}\left\{ I_0 \angle \theta \; e^{j\omega t} \right\}.$$

Finally, we can simplify the notation by dropping the *implied* $e^{j\omega t}$ term and the Re{} operator, leaving the *phasor notation*:

$$\mathbf{I} = I_0 \angle \theta \;\; = I_0 e^{j\theta} \;\; = I_0 (\cos\theta + j\sin\theta)$$

where the boldface **I** reminds us that the *phasor* quantity **I** is a complex number.

Let's use these ideas to re-analyze the circuit of Figure 2.1. We first replace the voltage source by the complex exponential expression $V_M e^{j\omega t}$. Since we know that the resulting current must also be sinusoidal, we can represent the current as the complex exponential $I_M e^{j(\omega t+\phi)}$, where I_M is the unknown amplitude of the current and ϕ is the unknown phase (relative to the phase of the source). The differential equation becomes

$$V_M e^{j\omega t} = R \cdot I_M e^{j(\omega t+\phi)} + \frac{1}{C}\int I_M e^{j(\omega t+\phi)}\, dt .$$

Performing the integral and regrouping,

$$V_M e^{j\omega t} = I_M e^{j\phi} e^{j\omega t} \cdot \left(R + \frac{1}{j\omega C} \right) .$$

Note again that both sides of this equation have an $e^{j\omega t}$ factor. Rewriting in phasor notation gives

$$\mathbf{V} = \mathbf{I} \cdot \left(R + \frac{1}{j\omega C} \right) .$$

Now solving for the phasor current,

$$\mathbf{I} = \frac{\mathbf{V}}{R + \frac{1}{j\omega C}} = \frac{V_M \angle 0°}{R - j\frac{1}{\omega C}} = \frac{V_M \angle 0°}{\sqrt{R^2 + \left(\frac{1}{\omega C}\right)^2} \angle -\tan^{-1}\frac{1}{\omega CR}}$$

$$= \frac{V_M}{\sqrt{R^2 + \left(1/\omega C\right)^2}} \angle \tan^{-1}\frac{1}{\omega CR}$$

As the final step we convert from phasor notation back to the time-domain current by reintroducing the real part of the time dependence (cos(ωt)), yielding

$$i(t) = \frac{V_M}{\sqrt{R^2 + \left(1/\omega C\right)^2}} \cdot \cos\left(\omega t + \tan^{-1}\frac{1}{\omega CR}\right),$$

which is the same result (*whew!*) as was obtained with the differential equation approach. The important advantage of this approach is that the mathematics involves mostly simple algebraic operations on the magnitudes and phases.

It is important to notice that the use of phasors and complex exponentials is based on the *cosine* function because the cosine is associated with the real part via Euler's equation. To represent a real *sine* function we need to include the 90° phase difference between the cosine and sine functions, i.e.,

$$K \cdot \cos(\omega t \pm \theta) \;\Leftrightarrow\; K\angle \pm \theta$$

but

$$K \cdot \sin(\omega t \pm \theta) \;\Leftrightarrow\; K\angle \pm \theta - 90°.$$

Impedance

It is interesting to examine these elementary voltage and current results. If we look at the complex ratio of phasor voltage and phasor current for each of the basic circuit elements we find:

Resistor, R: $$\frac{\mathbf{V}}{\mathbf{I}} = R$$

Inductor, L: $$\frac{\mathbf{V}}{\mathbf{I}} = j\omega L = \omega L\angle 90°$$

Capacitor, C: $$\frac{\mathbf{V}}{\mathbf{I}} = \frac{1}{j\omega C} = -j\frac{1}{\omega C} = \frac{1}{\omega C}\angle -90°$$

The **V**/**I** complex ratio is called the *impedance*, often denoted by the symbol **Z**. The units of impedance are ohms, since the ratio of volts to amps is defined to be ohms. The

impedance of a resistor is a purely *real* number with no frequency dependence: the resistance. The impedance of inductors and capacitors, however, is a purely *imaginary* number that *varies with the sinusoidal driving frequency* (ω): jωL and 1/jωC, respectively. A circuit containing a combination of resistors, capacitors, and/or inductors will, in general, have a *complex* impedance.

The really useful thing about analyzing networks in terms of impedance is that nearly all the techniques that apply to resistive circuits (KVL, KCL, parallel and series combinations, Thévenin and Norton equivalents, etc.) can be extended directly to impedances. For example, the total impedance of the circuit in Figure 2.2 can be determined by using a parallel combination of the individual impedances.

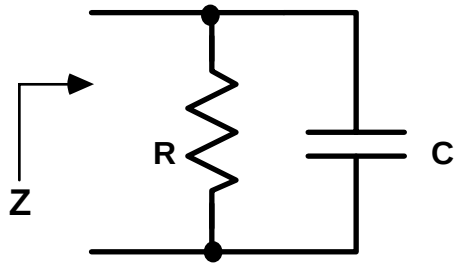


Figure 2.2

$$\mathbf{Z} = \mathbf{Z}_R \parallel \mathbf{Z}_C = \frac{\mathbf{Z}_R \cdot \mathbf{Z}_C}{\mathbf{Z}_R + \mathbf{Z}_C} = \frac{R}{1 + j\omega CR}$$

$$= \frac{R}{\sqrt{1 + (\omega CR)^2}} \angle -\tan^{-1} \omega CR$$

Notice that since **Z** is the complex ratio of **V**/**I**, the impedance gives the magnitude and phase relationship directly.

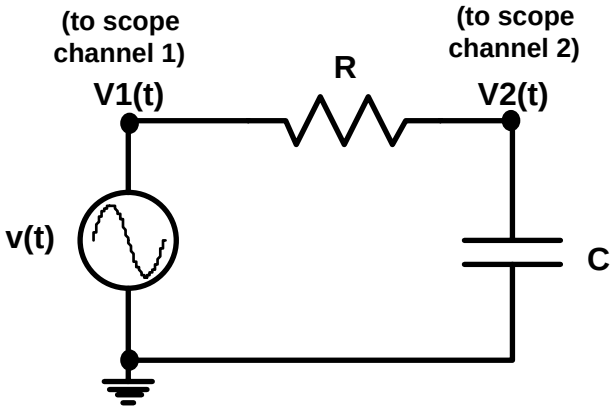
Measuring Impedance Magnitude and Phase

In order to measure the impedance of a circuit or circuit element we need to determine the magnitude and phase relationship of the input voltage and input current. This measurement can be accomplished using a dual channel oscilloscope.

Since the oscilloscope is a voltage measurement device, how can we use the 'scope to measure current? One way is to determine the voltage across a known circuit element (usually a resistor for convenience) and then to calculate the current via Ohm's law. Measuring the magnitude of voltages and currents is simple: just read the waveform amplitude off the 'scope display. Measuring the phase relationship is a bit more complicated since we need to see the *time* relationship between two waveforms. There are several methods to measure phase, as described below.

- Phase measurement using time difference

  One way to measure the phase difference between two signals with the same frequency is to set the 'scope for dual trace operation, trigger on the input or reference source, and observe the time difference between the reference waveform and the waveform measured at the desired node in the circuit. This is depicted in Figure 2.3.



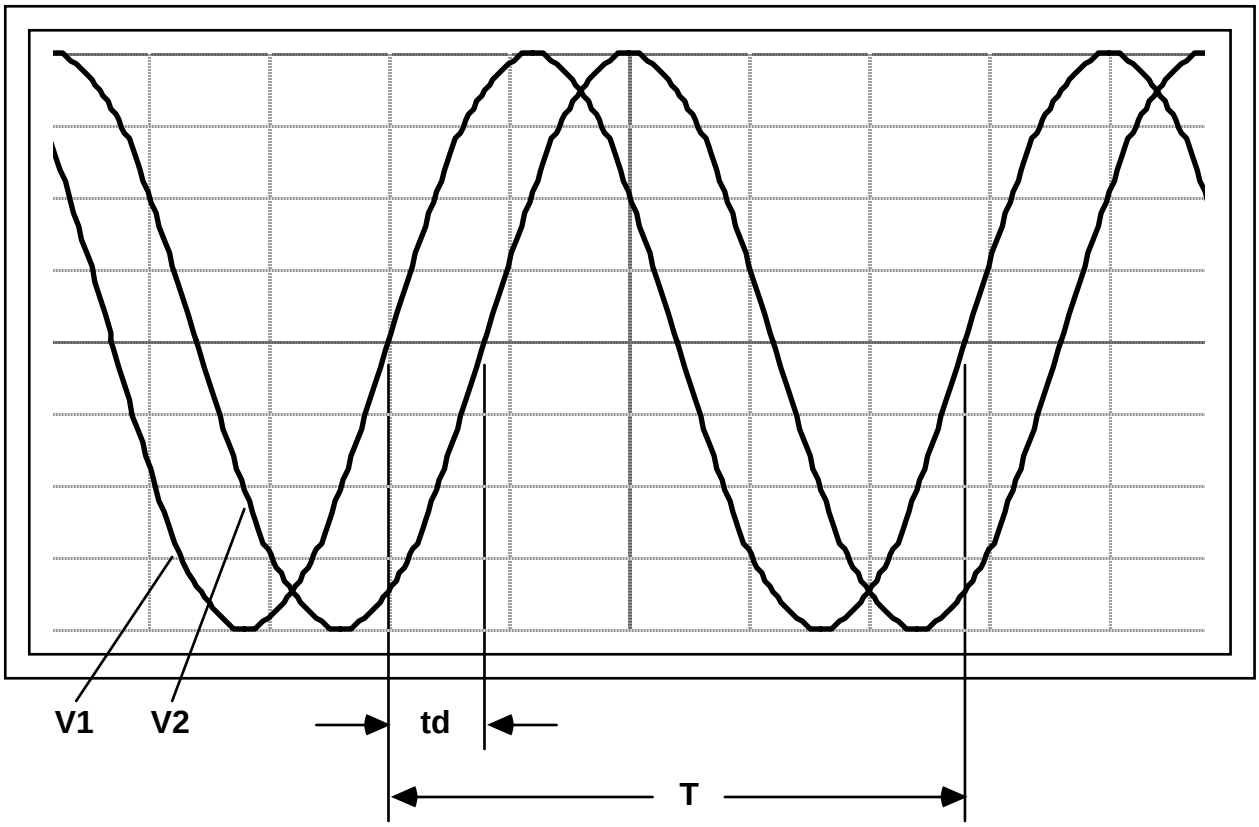


Figure 2.3

The phase difference between the two voltages is $2\pi \cdot (t_d/T)$ radians, or $360° \cdot (t_d/T)$ degrees.

- Phase measurement using Lissajous figures

Another way to determine the phase difference between two sinusoids is to make use of the X-Y capability of the oscilloscope. In this technique, the reference sinusoid is applied to the horizontal (X) deflection of the 'scope display while the other sinusoid is applied to the vertical (Y) deflection. Since the two waveforms have the same frequency but possibly differing phases, the resulting display will be an *ellipse*. For example, if the two waveforms are *in phase* they will both reach their maxima and minima at the same time, giving a straight diagonal line (a "squashed" ellipse). If, on the other hand, the two waveforms are 90° out of phase, the maxima and minima of one waveform always occur when the other waveform is zero, giving an ellipse with its primary axis running either horizontally or vertically depending upon the amplitude relationship of the two signals. Other phase differences give elliptical displays with various

orientations. These patterns, named in honor of the French mathematician Lissajous (pronounced LEE´-ZA-SHOO´), are known as *Lissajous figures*. Several examples are shown in Figure 2.4.

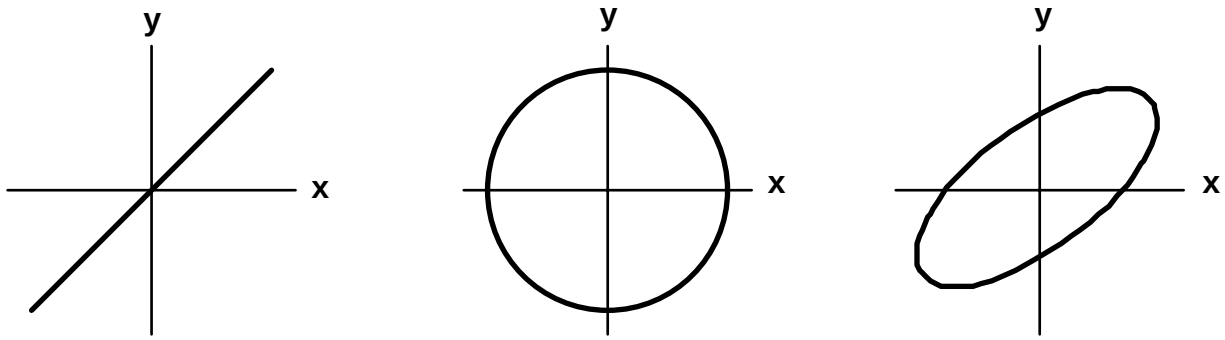


Figure 2.4

The phase difference ϕ between the two signals can be determined as follows. Let $x = A \sin \omega t$ and $y = B \sin(\omega t + \phi)$,

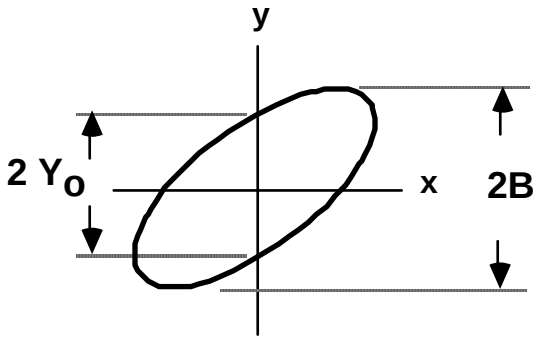


Figure 2.5

and from Figure 2.5 we see that when $x = 0$, $|y| = B \sin \phi = Y_o$, i.e., when $x = 0$, ωt must be a multiple of π. Therefore, the phase difference is given by

$$\sin \phi = \frac{Y_o}{B}, \quad \text{or} \quad \phi = \sin^{-1} \frac{Y_o}{B}$$

NOTE that if the phase difference exceeds 90° the Lissajous ellipse is tilted the other way (\), and the formula must be modified to $\phi = 180° - \sin^{-1} Y_o/B$.

- Phase measurement using the "sum and difference" method

Still another way to determine the phase difference between two sinusoids is to make use of the *differential input* capability of the oscilloscope. The differential input mode allows the 'scope to display the sum (CH1+CH2) or difference (CH1-CH2) of the vertical trace *deflections* of the two input channels. If the vertical deflection settings (volts/div) are the same for both input channels, then the display shows the algebraic sum or difference of the two input signals in volts.

If the two input signals have the *same amplitude and frequency* but differ in phase, we can determine the phase difference as follows:

Let $x = A \sin \omega t$

$y = A \sin(\omega t + \phi)$,

giving

$$x + y = A\left[\sin \omega t + \sin(\omega t + \phi)\right] = A\left|\sin\left(\omega t - \frac{\phi}{2}\right) + \sin\left(\omega t + \frac{\phi}{2}\right)\right| = 2A \cos\frac{\phi}{2} \sin \omega t$$

$$x - y = A\left[\sin \omega t - \sin(\omega t + \phi)\right] = A\left|\sin\left(\omega t - \frac{\phi}{2}\right) - \sin\left(\omega t + \frac{\phi}{2}\right)\right| = -2A \sin\frac{\phi}{2} \cos \omega t$$

Now if we measure the *amplitude* of the sum and difference signals we see that

$$\text{AMPL}(x + y) = \text{"SUM"} = 2A\cos\frac{\phi}{2}$$

and $$\text{AMPL}(x - y) = \text{"DIFF"} = 2A\sin\frac{\phi}{2}.$$

Thus, the phase difference, ϕ, can be obtained by observing the amplitude of the sum and difference waveforms with the 'scope, then calculating

$$\phi = 2 \cdot \tan^{-1}\left(\frac{\text{DIFF}}{\text{SUM}}\right).$$

Since the two input signals are not generally equal in amplitude, it is necessary to adjust the vertical gain so that the two signals have the same trace deflection on the 'scope screen. This is most easily accomplished by first adjusting the input (calibrated) gain settings until the two signals are approximately the same amplitude, then performing a "fine" adjustment using the continuously variable gain knob (labeled CAL). Recall that since the 'scope adds and subtracts the trace

deflections, not the absolute voltages, we can simply count the number of divisions to determine the SUM and DIFF values for use in the DIFF/SUM ratio even without the calibrated gain settings.

Question: how can the sum and difference method be used if the phase difference exceeds 90°?

REFERENCES

See Chapter 9 of the text by J. David Irwin, *Basic Engineering Circuit Analysis*, 4th ed., Macmillan Publishing Co., 1993 (pp. 382-424).

EQUIPMENT

Lab component kit	Ohm meter	Capacitance meter
Function generator	Oscilloscope	

PRE-LAB PREPARATION

(I) Determine the impedance of the following circuit elements at 0 Hz, 100 Hz, 1 kHz, and 10 kHz. Express the impedances in both rectangular and polar form.

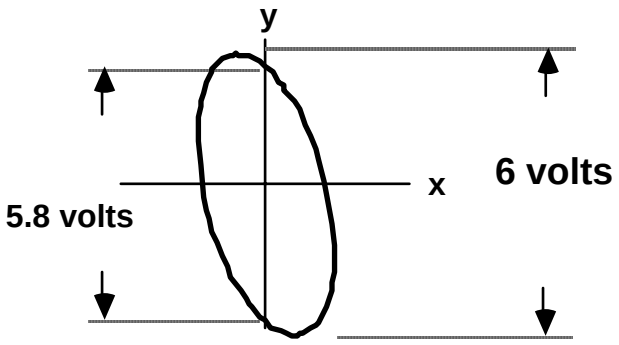
a) 100Ω resistor b) 0.1μF capacitor c) 0.3H inductor

(II) For the circuit of Figure 2.1, determine a mathematical formula for the voltage across the capacitor in terms of R, C, V_M, and ω.

(III) Determine the phase difference between sinusoidal signals for these two different cases:

a) Sum and difference method: SUM = 7.5 units, DIFF = 1.5 units.

b) Lissajous method:



EXPERIMENT

(1) Construct the series RC circuit of Figure 2.1. Use the bench function generator, a nominal 220Ω resistor and a nominal 0.1μF capacitor. Remember to measure and record the actual values of the components used.

Choose an appropriate AC signal amplitude, V_M (large enough to display easily with the 'scope but within the power limitations of the resistor used). Setup the 'scope so that measurements of the input voltage and current can be made (or calculated easily).

Determine the magnitude and phase of the series RC impedance over at least the frequency range 200Hz thru 200kHz. NOTE that you can determine the current from measurements across the resistor using Ohm's law (i=v/R). Try a few of the measurements with each of the phase determination methods described previously to see which technique seems most convenient and reliable. Measure the impedance at enough different frequencies to determine the behavior of the impedance magnitude and phase. *Be sure* to verify the signal frequency with the oscilloscope (the markings on the function generator dial may not be extremely accurate). Also, be sure to measure the function generator output at each frequency since the output amplitude from the generator may be different at different frequencies!

It is traditional and convenient to plot the impedance-vs.-frequency data on a *logarithmic* frequency scale (base-10). A good starting point is to measure and plot the data at an approximately equally-spaced log scale, such as 200Hz, 500Hz, 1kHz, 2kHz, 5kHz, 10kHz, etc. Note that the "1, 2, 5" spacing results in roughly equal base-10 logarithmic steps. Be sure to take additional measurements if the data plot turns up any "interesting" features (bends, peaks, etc.).

(2) Now replace the nominal 220Ω resistor with a 1kΩ resistor and again determine the impedance over the same frequency range as before. Use the phase measurement technique that you found to be the most straightforward in part 1.

RESULTS

(a) Prepare a plot of the impedance phase measurements made in part 1 of the experiment. Show the data as a semi-log plot: phase in degrees (linear scale) versus frequency (logarithmic scale). On the same plot show the mathematical prediction for the phase, i.e., determine the impedance of the series RC circuit. Discuss the results. Which of the phase measurements seemed to work the best for you? Why?

(b) Prepare two plots of the impedance magnitude measurements made in part 1. For the first plot, show the magnitude measurements along with the mathematical prediction as a semi-log plot: magnitude in ohms (linear scale) versus frequency (log scale). For the second plot, again show the measured and calculated magnitude values but use a log-log plot: magnitude (log scale) versus frequency (log scale). Discuss the results and compare the features of the two data plots.

(c) Prepare a plot of the impedance phase measurements (semi-log) and a plot of the impedance magnitude measurements (log-log) from part 2. On the same plots show the mathematical predictions for the impedance. Discuss the differences between the plots for part 1 and the plots for part 2.

(d) What would you change about the procedures of this experiment?

Revised 7/94

Lab # 3
TITLE: Impedance II: Input Impedance and Active Circuits

ABSTRACT

The AC steady-state analysis techniques developed in the previous lab experiment are used to characterize several electronic circuits. The use of circuit simplification techniques and equivalent circuits are explored, leading to the concept of *input impedance* and *output impedance*. The description of an an active electrical circuit in terms of impedances is also introduced.

INTRODUCTION AND THEORY

As considered in Lab #2, the sinusoidal steady-state *impedance* is defined as the complex ratio of voltage to current measured between two points within an electrical network. Furthermore, the basic circuit analysis procedures taught in EEngr 213 can be extended directly to the sinusoidal steady-state situation.

One common use of the impedance concept is in the simplification of complex electrical networks into a Thévenin equivalent impedance and voltage source. The main difference between the Thévenin circuit for a resistive network and the more general Thévenin "impedance" circuit is that the impedance varies with frequency.

Input Impedance

Consider the situation depicted in Figure 3.1. Here, a circuit consisting of only unknown passive linear elements (resistors, capacitors, and inductors) is contained in a "black box" that is accessible only by two wires. Let's assume that the two wires represent the *input* to the circuitry contained in the black box, e.g., the input to an audio amplifier or the connections to an electric motor.

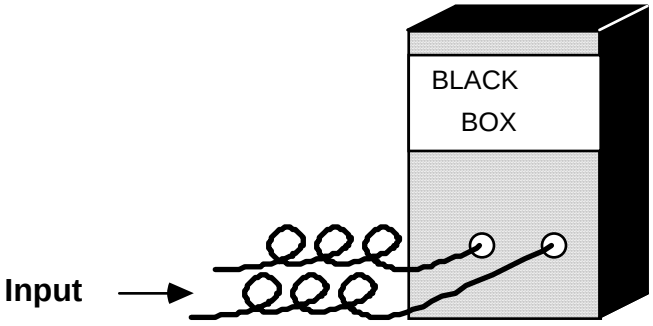


Figure 3.1

What we really want to determine is the impedance in the box measured between the two input wires: the *input impedance*.

One way to determine the input impedance is to attach a known voltage source between the inputs and measure the resulting input current, as shown in Figure 3.2 (complex ratio $\mathbf{Z}_{in} = \mathbf{V}_{in}/\mathbf{I}_{in}$).

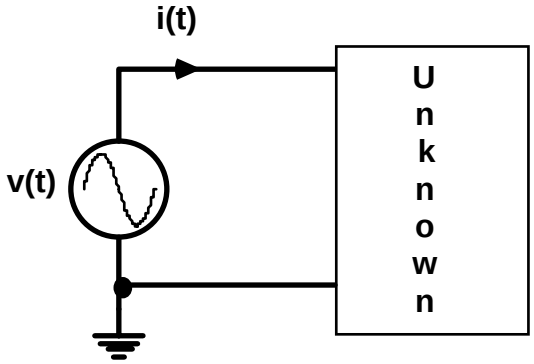


Figure 3.2

Measurements can be made at a range of different input frequencies if the frequency dependent characteristics of the impedance is desired. Note that in an actual measurement a series resistor is typically included so that the input current can be displayed using an oscilloscope, as in Lab #2. It it also important to note that this input impedance measurement procedure applies for PASSIVE networks only (no sources in the black box).

Output Impedance

Another similar situation—but now allowing an internal sinusoidal signal source—involves determination of the *output impedance* of an electrical network. The output impedance is defined as the Thévenin impedance of the network measured between the two output connections. This concept is shown in Figure 3.3.

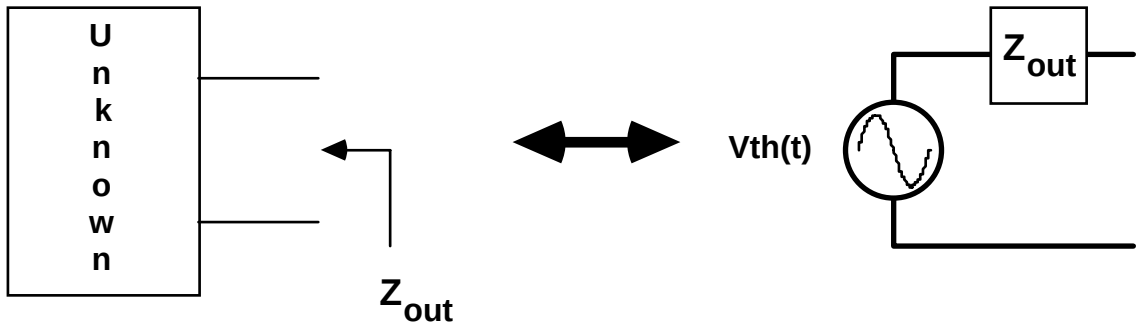


Figure 3.3

For example, we might be interested in determining the output impedance of a 120Vrms power outlet. Between the generating station (where $V_{th}(t)$ is located) and the wall outlet there are likely to be miles of transmission lines, transformers, resistive losses, stray capacitances, etc. Since it is generally impractical to measure all the individual impedances between the generator and the outlet, we would rather simplify the network and lump all the effects into a *single* output impedance, Z_{out}, that can be measured directly at the outlet.*

The Thévenin impedance (the output impedance in this case) is defined to be the complex ratio of the open circuit voltage and the short circuit current. In order to determine the Thévenin voltage we simply measure the open circuit voltage. However, the short circuit current presents several practical problems in attempting to determine the Thévenin impedance. First, we need the *phase* relationship between the voltage and current in the circuit, which means the two measurements must be made at the same time so that the relative phase can be determined. It is not possible to have both an open circuit and short circuit measurement at the same time. Second, even if we are only interested in the magnitude of the impedance and not the phase, it is often impractical to "short out" the circuit due to the large current that may flow if the output impedance is small. For example, in the 120V wall outlet mentioned in the previous paragraph, applying a short circuit to the output should cause the fuse or circuit

* Note that although many multimeters measure resistance, they are designed for use with *passive* circuits only (a small voltage source in the meter is used to pass a current through the components under test). Hooking such a meter to an *active* circuit (like a wall outlet) in order to measure resistance is not possible and can be dangerous.

breaker protecting the branch circuit to blow, or possibly an unsafe current could flow through the wall wiring if no fuse was present.

So how can we measure the Thévenin impedance? Instead of using the short circuit current, we can make voltage and current measurements with two known load impedances attached. It is usually most convenient to use two resistors for the loads, since the voltage and current are in phase for resistances. It is important to notice that we can accomplish a similar measurement by attaching a known voltage source and measuring the resulting current for two different voltages, since the resistors we attach as loads presumably obey Ohm's law.

Consider the circuit of Figure 3.4. Here we assume that the Thévenin source magnitude **V** has already been determined by an open circuit voltage measurement, and the source phase is arbitrarily set to zero. Since in general we cannot have access to the components and nodes inside the dotted box, we won't be able to determine the sign (impedance phase) of Z_{out} by measuring the phase difference between **V** and $\mathbf{V}_o$.

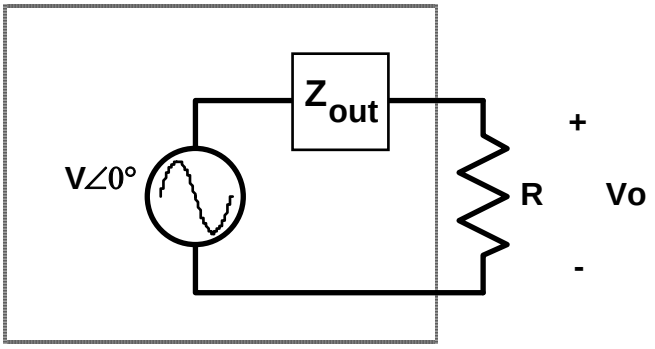


Figure 3.4

With the known load resistor, R, attached, the magnitude of the output voltage can be expressed by the voltage division relationship

$$|\mathbf{V}_o| = \frac{R}{|R + Z_{out}|}|\mathbf{V}| = \frac{R}{|R + R_{out} + jX_{out}|}|\mathbf{V}|$$

$$= \frac{R}{\sqrt{(R + R_{out})^2 + (X_{out})^2}}|\mathbf{V}| \quad .$$

Note that once we measure $|\mathbf{V}_o|$ we have an expression with two unknowns: R_{out} and X_{out}, the resistive and reactive parts of the output impedance, respectively. Since we have two unknowns, we need another equation to solve simultaneously. The second equation can be obtained by making a second measurement with a different known resistor attached as a load. Naming the two load resistors R_1 and R_2 and the corresponding output voltage measurements V_{o1} and V_{o2}, the resulting equations can be written:

$$\begin{cases} \sqrt{(R_1 + R_{out})^2 + (X_{out})^2} = R_1 \dfrac{|\mathbf{V}|}{|\mathbf{V}_{o1}|} \\ \sqrt{(R_2 + R_{out})^2 + (X_{out})^2} = R_2 \dfrac{|\mathbf{V}|}{|\mathbf{V}_{o2}|} \end{cases}.$$

Squaring both sides of both equations, then subtracting, gives

$$(R_1 + R_{out})^2 - (R_2 + R_{out})^2 = \left(R_1 \frac{|\mathbf{V}|}{|\mathbf{V}_{o1}|} \right)^2 - \left(R_2 \frac{|\mathbf{V}|}{|\mathbf{V}_{o2}|} \right)^2$$

Rewriting the left side (difference of two squares) as

$$(R_1 + R_{out})^2 - (R_2 + R_{out})^2 = (R_1 + R_2 + 2R_{out}) \cdot (R_1 - R_2)$$

and solving for R_{out} results in:

$$R_{out} = \frac{1}{2(R_1 - R_2)} \cdot \left[\left(R_1 \frac{|\mathbf{V}|}{|\mathbf{V}_{o1}|} \right)^2 - \left(R_2 \frac{|\mathbf{V}|}{|\mathbf{V}_{o2}|} \right)^2 \right] - \frac{(R_1 + R_2)}{2}$$

Finally, $|X_{out}|$ can then be determined from either of the original equations, viz.:

$$(X_{out})^2 = \left(R \frac{|\mathbf{V}|}{|\mathbf{V}_o|} \right)^2 - (R + R_{out})^2$$

If it were possible to determine the phase relationship between the Thévenin source and the output voltage we could determine the sign of X_{out}, i.e., whether the reactance was capacitive (-) or inductive (+). Can you think of any other way we could determine the sign of X_{out} ?

Impedance and Active Circuits

It is also possible to describe op amp circuits in terms of AC sinusoidal analysis. For example, consider the basic inverting op amp configuration shown in Figure 3.5.

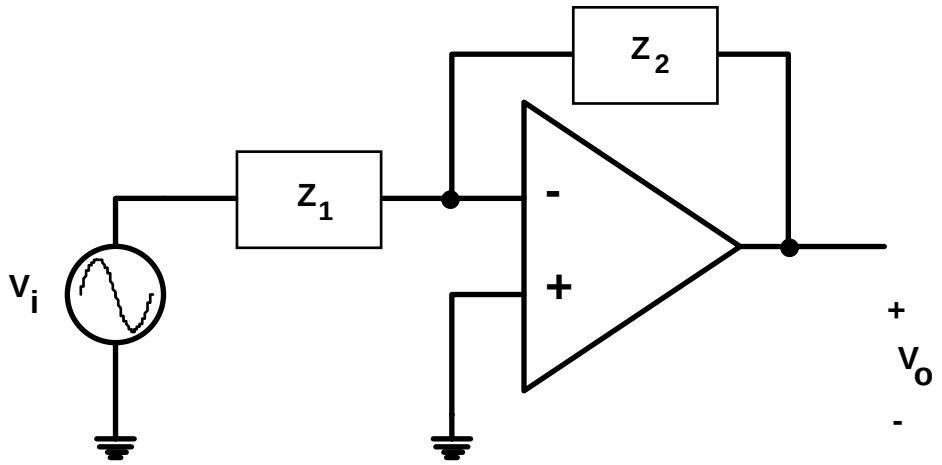


Figure 3.5

Analysis of this circuit using the basic ideal op amp properties considered in EEngr 213 shows that the phasor relationship for the circuit is given by

$$\mathbf{V}_o = -\frac{\mathbf{Z}_2}{\mathbf{Z}_1}\mathbf{V}_i$$

.

It is also possible to determine the input impedance and output impedance for the circuit. The input impedance ($\mathbf{V}_i/\mathbf{I}_i$) is simply $\mathbf{Z}_1$ because the input voltage appears entirely across $\mathbf{Z}_1$ (the inverting op amp input is held at ~0 volts). The output impedance is *zero*, since the output impedance of the op amp (ideal) is itself zero (the parallel combination of zero with anything else is still zero)! Of course, a real op amp is not completely ideal so the input and output impedances only approach the ideal values.

REFERENCES

See Chapter 9 of the text by J. David Irwin, *Basic Engineering Circuit Analysis*, 4th ed., Macmillan Publishing Co., 1993 (pp. 382-424).

EQUIPMENT

Lab component kit	Ohm meter	Capacitance meter
Function generator	Oscilloscope	

PRE-LAB PREPARATION

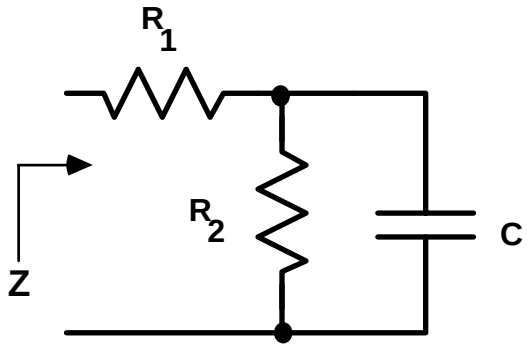


Figure 3.6

(I) Determine an expression for the input impedance of the series-parallel network in Figure 3.6. What is the input impedance (magnitude and phase) for low frequencies ($\omega \varnothing 0$) and for high frequencies ($\omega \varnothing \square$)?

(II) The circuit of Figure 3.6 is attached to a sinusoidal voltage source, as shown in Figure 3.7. The circuit is configured with: $|\mathbf{V}| = 1$ volt, $\omega = 2\pi \cdot (10\text{kHz})$, R_1=1kΩ, and R_2=10kΩ. The value of the capacitor is unknown, but the amplitude of the voltage across the capacitor is measured to be 0.707 volts. From this single measurement, determine the value of the capacitance and the expected phase difference between the input voltage waveform and the input current waveform.

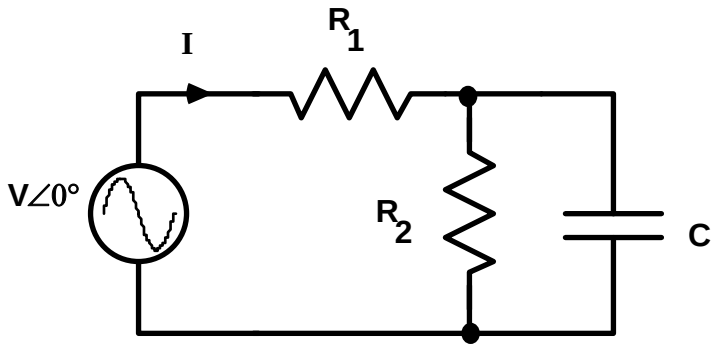


Figure 3.7

(III) What is voltage gain expression ($\mathbf{V}_o/\mathbf{V}_i$) for the circuit of Figure 3.8? Assume an ideal op amp. Calculate the magnitude and phase of the gain expression for frequencies from 10Hz to 100kHz using a "1, 2, 5,..." frequency sequence (use a computer program or MAPLE, if you wish). Finally, use PSpice to perform an AC analysis of the circuit over the 10Hz - 100kHz range. Use the PSpice `ua741` op amp model. Plot the PSpice magnitude results on a log scale with a log frequency axis.

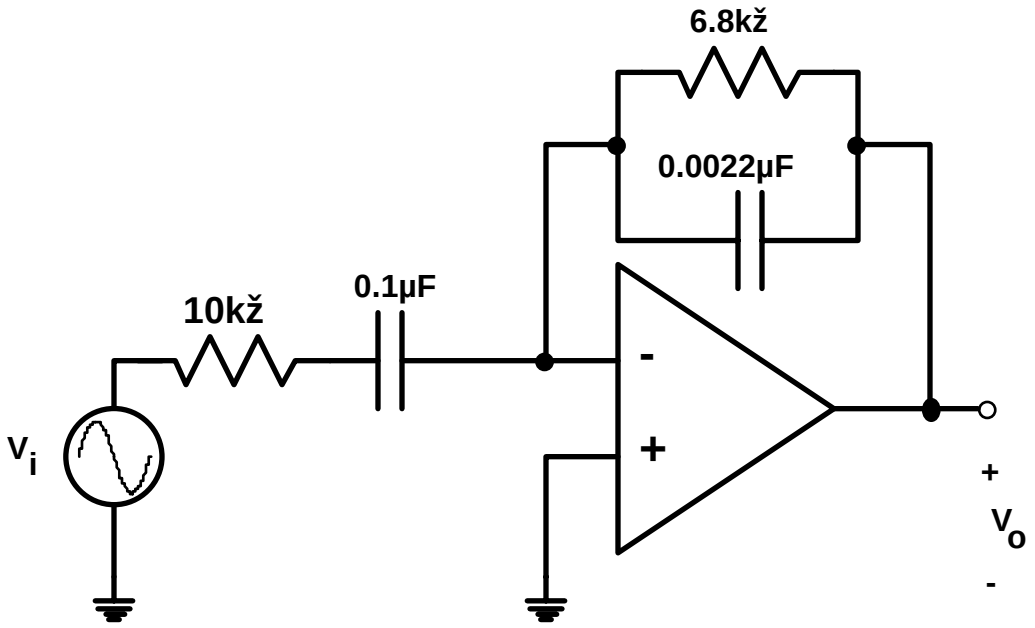


Figure 3.8

EXPERIMENT

(1) Assemble the circuit of Figure 3.7 using the function generator as the source and the nominal component values R_1= 1kΩ, R_2= 10kΩ, and C= 0.1μF. Make measurements of the impedance magnitude and phase at enough frequencies to fully describe the behavior of the circuit.

(2) Now assume that the circuit of Figure 3.7 is an *unknown* circuit that you can access only via two wires, as show in Figure 3.9 below. Set the generator for 2 volts peak-to-peak at 2kHz. Using the "load resistor" approach described in the lab introduction, make external measurements of your choice to come up with an estimate of the Thévenin equivalent circuit for the network as observed from the external connections.

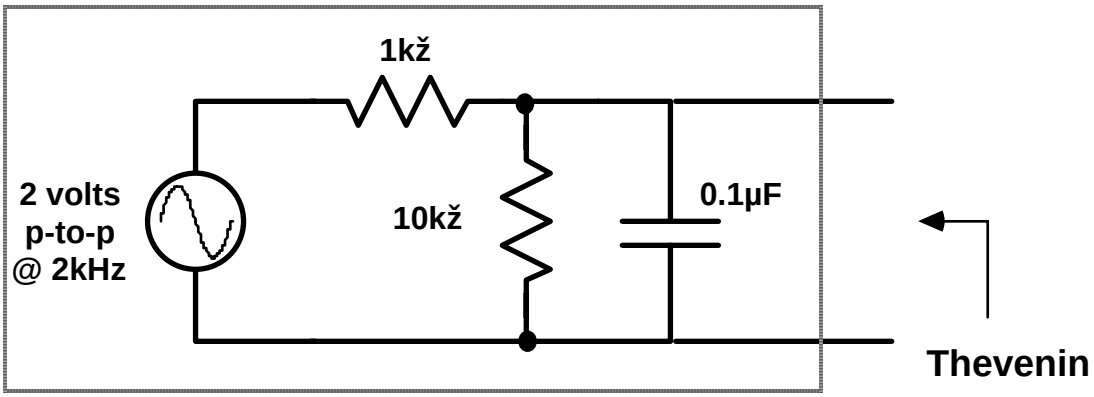


Figure 3.9

(3) Assemble the circuit of Figure 3.8 using the indicated nominal component values. Measure the complex voltage gain ($\mathbf{V}_o/\mathbf{V}_i$), both magnitude and phase, over the frequency range 10Hz thru 100kHz. Take sufficient measurements to fully describe the behavior of the circuit.

RESULTS

(a) Prepare a plot of the impedance magnitude and phase using the measurements of part 1. Also plot the theoretical prediction of the impedance using the measured component values in the mathematical expression for the impedance developed in the pre-lab. Use a log scale for the frequency axis, plot the magnitudes on a log scale, and plot the phases on a linear scale. Discuss the results.

(b) What load resistor values did you use in your measurements for part 2? Compare your measured Thévenin impedance results to a theoretical prediction based on the known circuit configuration.

(c) Plot your magnitude and phase measurements of the voltage gain from part 3 and compare with the mathematical expression (ideal op amp) and PSpice results from the pre-lab. Again, use a magnitude (log axis) vs. frequency (log axis) plot.* How would you describe the agreement between the measurements and the predictions?

(d) How would you modify this experiment to make it more useful to you?

Revised 7/94

* Incidentally, this form of plot (log gain vs. log frequency) is referred to as a *Bode* (Boh-dee) plot, named after the engineer H. W. Bode.

Lab # 4
TITLE: Terminal Characteristics of Semiconductor Diodes

ABSTRACT

The *diode* is the most commonly encountered nonlinear circuit element. This experiment involves measurements of the voltage and current behavior of a semiconductor diode, and the behavior of several electrical networks involving resistors and diodes. The measured results are compared to SPICE simulations and hand analysis using elementary diode models.

INTRODUCTION AND THEORY

Like resistors, inductors, and capacitors, the semiconductor diode is a passive two-terminal device. But unlike R, L, and C, the diode is a *nonlinear* circuit element, meaning that the relationship between voltage and current in the diode will not be linear in a mathematical sense. This means that some of our basic circuit analysis techniques, such as superposition and proportionality, will *not* be applicable to diode circuits. The implications of nonlinear circuit analysis will be explored in this and subsequent experiments.

Characteristics of Diode Behavior

The diode is a physical approximation to a unidirectional wire: an ideal diode would be a perfect conductor for one direction of current through the device, and a perfect insulator for current attempting to flow in the other direction. Such an ideal device could also be described as having zero impedance in one direction and infinite impedance in the other direction. The schematic symbol for a diode is depicted in Figure 4.1a. Forward (positive) current enters at the *anode* of the device and exits at the *cathode*.

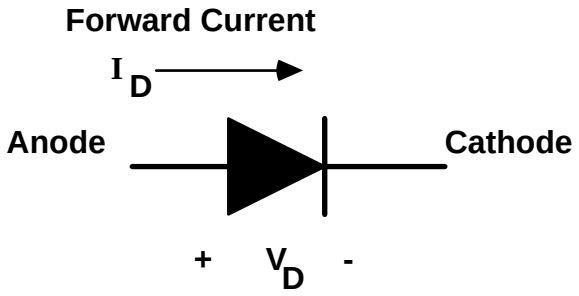


Figure 4.1a

If the circuit attached to the diode results in current through the diode in the *forward* direction (with the arrow) the diode is said to be *forward biased*, or simply *ON*. If the circuit attached to the diode attempts to force current in the reverse direction, the diode is said to be *reverse biased*, or *OFF*. A plot of the terminal characteristics (current vs. voltage) for an ideal diode is shown in Figure 4.1b.

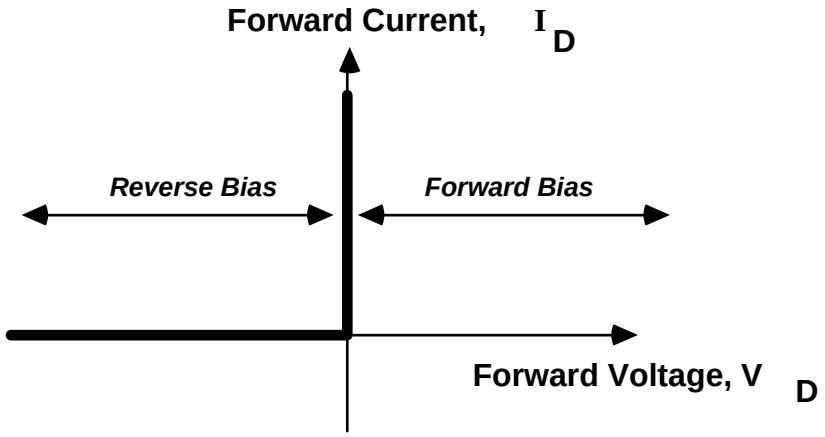


Figure 4.1b

Note that if it were possible to construct an ideal diode, it would conduct any amount of current with zero voltage drop (vertical line on V=0, I>0 axis) and zero current with any amount of reverse bias voltage (horizontal line on I=0, V<0 axis). Although such an ideal device does not exist, the ideal diode concept is useful in performing a quick "eyeball" analysis of a real diode circuit.

A real semiconductor diode (or *junction diode*[*]) has terminal characteristics which differ from the ideal case in several respects, as shown in Figure 4.2. A semiconductor diode

[*] The term *junction* diode comes from the fact that the diode is constructed as a metallurgical junction between two materials with different electrical properties, such as p- and n-type semiconductors.

fabricated from silicon materials requires a forward bias of approximately 0.7 volts before the device conducts appreciably in the forward direction. In the reverse direction the diode conducts a small *leakage* current that is usually much smaller than the forward current. The junction diode is typically composed of a *pn junction*, meaning that *p*-type and *n*-type semiconductor materials are fabricated in direct contact with each other. The anode of the device is *p*-type material and the cathode is *n*-type. Thus, the *forward* current through the device is in the direction from *p* to *n*.

Analysis of the physical mechanisms for current conduction across semiconductor junctions (considered in EEngr 315, etc.) gives a theoretical description of the voltage and current relationship in a real junction diode:

$$I_D = I_s\left(e^{\frac{V_D}{nV_T}} - 1 \right),$$

where

I_D and **V_D** are the diode current and voltage as defined in Figure 4.1,
I_s is the *scale current*,
V_T is the *thermal voltage*,
and **n** is a constant between 1 and 2.

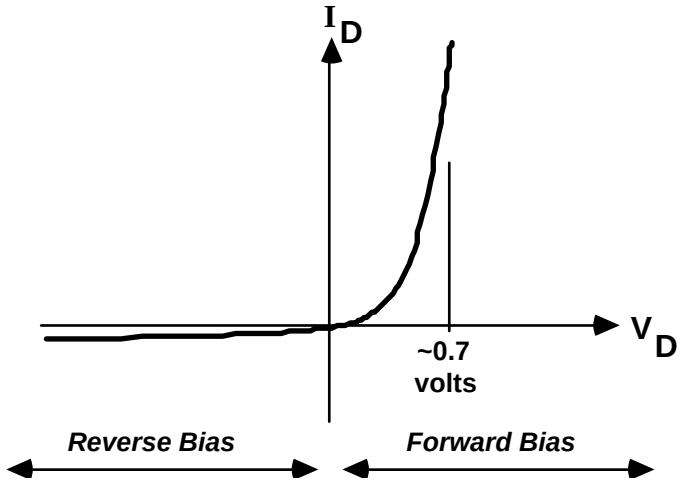


Figure 4.2

The scale current I_s is a constant for a particular diode at a fixed temperature, but varies with the size and temperature of the junction. Typical values of I_s for small diodes are in the range of 10^{-13} to 10^{-15} amps. V_T, the thermal voltage, is defined as kT/q, where k

is Boltzmann's constant (1.38×10^{-23} joules/kelvin), T is the absolute temperature in kelvin, and q is the charge of an electron (1.602×10^{-19} coulomb). Near room temperature V_T is approximately 25mV. Finally, the constant n ($1 \le n \le 2$) depends upon the material used to make the diode and the physical geometry of the device.

The diode equation predicts that the reverse current (current flowing under reverse bias conditions) should be equal to I_S. In a real diode, however, additional *leakage* current is usually present due to the packaging of the diode and other effects so that the reverse current may be many times greater than predicted by semiconductor theory.

If the reverse voltage is increased above some particular value the diode will exhibit *reverse breakdown*. In the breakdown region the diode no longer behaves as an open circuit, and appreciable current may flow in the reverse direction through the device. This behavior is sketched in Figure 4.3. Although operation in the breakdown region is not necessarily damaging to the diode, the *power dissipation* ($I_{reverse} \cdot V_{reverse}$) must be limited so that the device does not burn up.

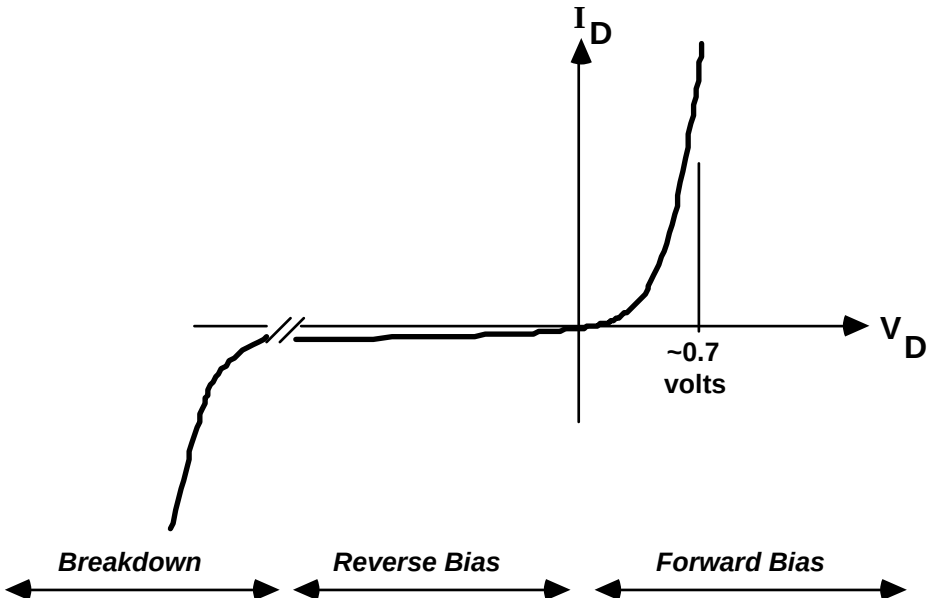


Figure 4.3

Zener Diodes

Some diodes are designed specifically to operate in the breakdown region. These devices are called *breakdown diodes*, or more commonly *Zener diodes* (ZEE-NUR), named for a semiconductor researcher. Zener diodes are designed to have a very abrupt

transition from the reverse bias region to the breakdown region and a very steep slope (current vs. voltage) in the breakdown region. This allows the Zener diode to be a good voltage reference when operated in the breakdown region (holding an essentially constant voltage for small variations in current). Zener diodes behave like "regular" diodes when operated in the forward bias region. Zeners are available with breakdown voltages from a few volts to a few tens of volts. The symbol for a Zener diode is shown in Figure 4.4.

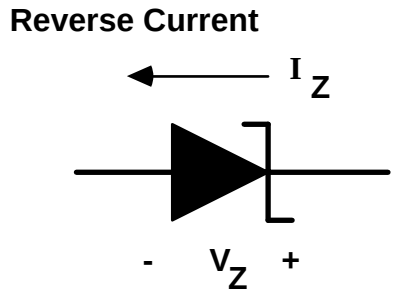


Figure 4.4

Note that the voltage and current specifications for Zeners are usually given for the *reverse* direction, i.e., operation in the breakdown region. The power dissipation rating for Zener diodes must be obeyed to prevent damage to the device. This usually means the inclusion of a series resistance in the circuit to limit the Zener current in the breakdown region.

Diode Specifications

Ordinary junction diodes can be classified roughly into two general types: *switching* diodes for use in low-power signal processing applications, and *power* diodes for use in electrical power circuits. Discrete diodes are rated by manufacturers using several parameter specifications, as summarized below.

- *Maximum forward average current ($I_{F(AV)}$)* - this specification indicates the allowable average current the device is designed to handle without being damaged. A *peak* or *surge* current rating is sometimes also given, indicating the maximum current capability of the device for a short period of time (usually a few milliseconds at most).

- *Maximum peak reverse voltage ($V_{R(PEAK)}$)* or *peak inverse voltage (PIV)* - this specification gives the maximum voltage that can be applied in the reverse

direction across the diode. Exceeding this voltage can result in diode breakdown, which means that appreciable current will start to flow in the reverse direction through the device.

- *Maximum forward voltage at specified current ($V_{F(MAX)}$ @ I_F)* - the forward voltage at a specified current identifies how much voltage drop we can expect across the diode when conducting in the forward direction. Sometimes a diode is referred to as an "*X* milliamp diode", where *X* is the nominal forward current when the diode voltage is 0.7 volts.

- *Reverse recovery time ($t_{rr(max)}$)* - when the diode is switched suddenly from the forward conduction state to the reverse blocking state a large reverse current is often observed for tens or hundreds of nanoseconds ($t_{rr(max)}$) before the diode begins to block the reverse current. This effect is due to the finite time required to move the charge carriers (electrons and holes) at the semiconductor junction. The reverse recovery effect is most noticeable for diodes with large junction area when switching state (on to off) in a rapid fashion, as depicted in Figure 4.5.

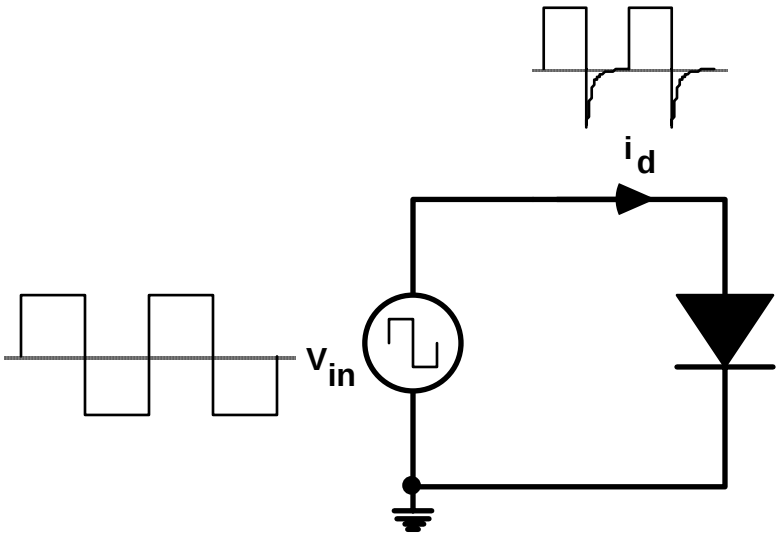


Figure 4.5

Diode Rectifiers

Diodes are used in numerous important applications in electrical engineering. Some of the most common applications are in *rectification*. Rectification allows an AC input signal (zero average value) to be converted to a time varying signal with a DC component (nonzero average value). This process is needed for using an AC power line

voltage to supply a DC voltage in a power supply. Consider the circuit of Figure 4.6. In this example the alternating voltage source attempts to create an alternating current in the loop.

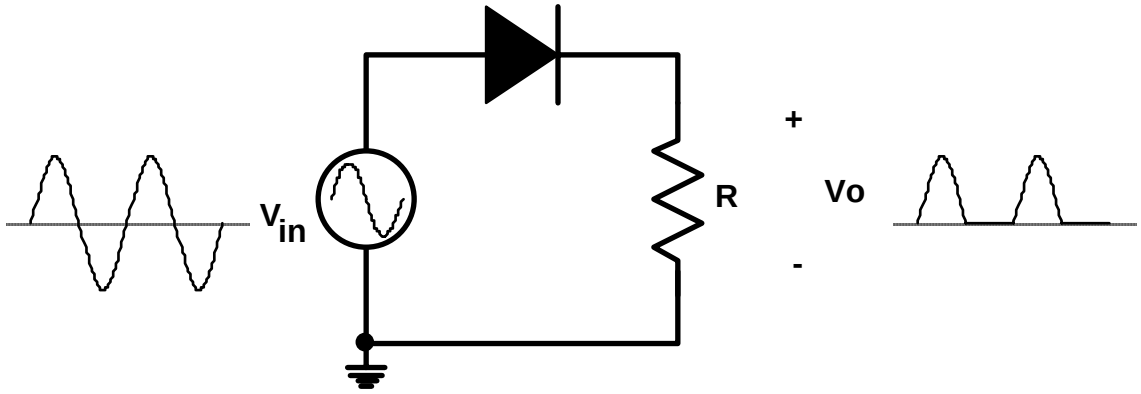


Figure 4.6

When the voltage at the source is positive, current will tend to flow through the diode in the forward direction, through the resistor, and back to the source. However, when the voltage at the source becomes negative, current would have to flow in the *reverse* direction through the diode, which is not possible. Since only current in the positive direction is allowed through the resistor the output voltage is only positive. This circuit performs *half-wave rectification* because only half of the input waveform appears at the load resistor. Because a real junction diode has a non-zero forward voltage when conducting ($V_D \approx 0.7$ volts), the output voltage will be less than the input voltage ($V_{o,\,peak} = V_{in,\,peak} - V_D$).

It is possible to create a *full-wave rectifier* using a diode *bridge* circuit, as shown in Figure 4.7.

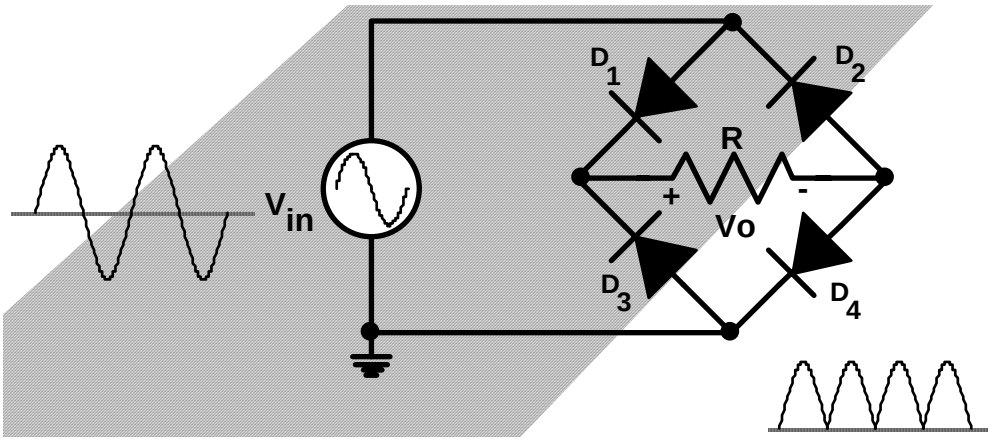


Figure 4.7

For positive source voltages the current flows through D_1, through the load resistor from left to right, through D_4, and back to the source (D_2 and D_3 are reverse biased and do not conduct). Similarly, when the source voltage goes negative the current is induced to flow through D_3, through the load *again from left to right*, through D_2, and back to the source. Thus, the current flows through the load in the same direction for both positive and negative input voltages, i.e., the *full-wave* is rectified. Note that a full-wave rectifier constructed as a diode bridge has a *floating load*, that is, the load resistor cannot be connected to the ground reference of the source (this would place a short circuit across one of the bridge diodes). Also notice that the voltage across the load is less than the input voltage by *two* diode "on" voltages since the load current must flow through two diodes.

Diodes and SPICE

SPICE includes a built-in diode model. The model implements the basic junction diode equation, except SPICE uses the symbol **IS** for I_S, and **N** for n. A diode is declared in SPICE as:

```
Dname   +node  -node  modelname
...
.MODEL  modelname  D  (IS=xx, N=yy),
```

where *+node* and *-node* are the node numbers connected to the anode and cathode of the diode, respectively. The name of the diode (*Dname*) is up to you, except that the first letter must be a D. You are also free to choose the name of the model.

The SPICE diode model also has numerous other parameters besides the basic diode equation. For example, the SPICE diode can simulate operation in the breakdown region, if desired.

Diode Packaging

Discrete diodes come in various shapes and sizes. The smallest discrete diodes are similar in size to 1/4-watt resistors, but are usually black in color or constructed from glass or colored plastic. The cathode of the diode is typically indicated by a wide band or some other marking, as shown in Figure 4.8. Power diodes are generally larger in size, and are often equipped with a large metal flange to allow the device to be physically mounted on a heat sink. Of course, it is always possible to verify the polarity of the diode simply by testing: The diode should conduct negligible current when in reverse bias and an approximately fixed voltage drop in the forward bias direction. Diodes are often given a standard part number beginning with '1N', e.g., 1N4001, 1N251, etc.

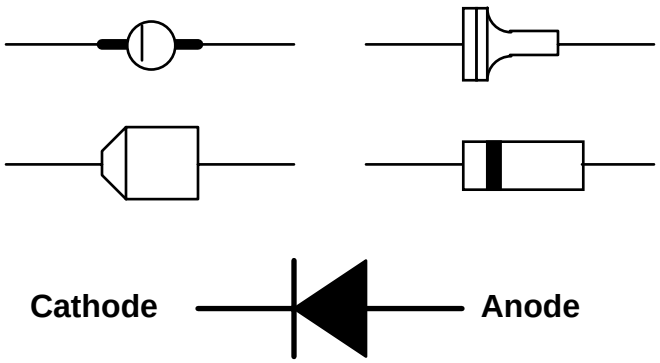


Figure 4.8

It is also possible to purchase bridge diode circuits consisting of several diodes mounted in a single package. These devices simplify the layout and assembly of rectifier circuits by reducing the number of individual components that must be handled.

REFERENCES

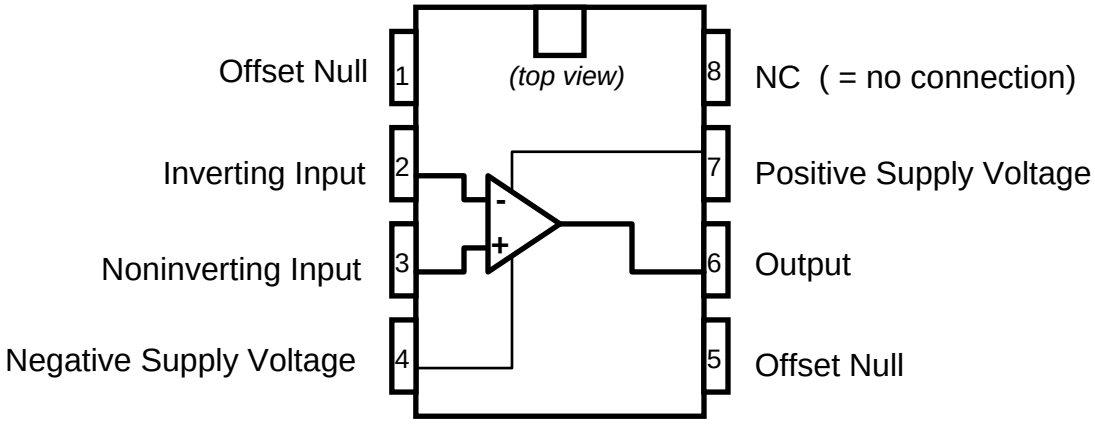
See Chapter 3 of the text by Sedra and Smith, *Microelectronic Circuits*, 3rd ed., Saunders College Publishing (Holt, Rinehart, and Winston), 1991 (pp. 116-190).

SPICE User's Guide, (available from UNL IEEE Student Branch)

Paul W. Tuinenga, *SPICE: A Guide to Circuit Simulation and Analysis Using PSpice*, 2nd Ed., Prentice-Hall, 1992.

EQUIPMENT

Lab component kit (resistors, op amp, and diodes) Curve Tracer
Digital Multimeter (DMM) Function generator Oscilloscope
Heathkit trainer



Type 741 op amp pinout

PRE-LAB PREPARATION

(I) A diode is connected in a circuit under forward bias conditions. Two measurements of the diode voltage and current are:

0.63 volts @ 10.1mA and 0.71 volts @ 110mA

From these measurements calculate the value of I_s and n for this diode. Assume the thermal voltage, V_T, is 25mV.

(II) A 20mA diode (V_D = 0.7 volts when I_D = 20mA) is known to have n=2. Use iteration or some other method and the junction diode equation to solve for the unknown loop current and diode voltage in the circuit of Figure 4.9 below. Also, simulate the circuit using SPICE and compare the results to your hand analysis.

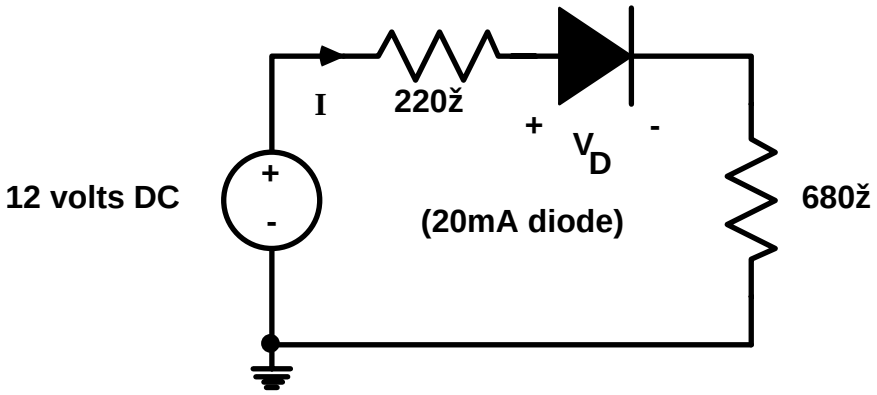


Figure 4.9

(III) A half-wave rectifier circuit is constructed as shown in Figure 4.6. Use an "ideal" diode model (short circuit for forward current, open circuit for reverse voltage). Using a 120V rms input sinusoid and R=10Ω, calculate the *peak* forward current and *peak* reverse voltage for the diode, the *average* forward current in the diode, and the *rms* power dissipated in the resistor. Recall that the average of a periodic signal, x(t), with period T is defined $\frac{1}{T}\int_{t_o}^{t_o+T} x(t)\,dt$, while the rms value is defined $\sqrt{\frac{1}{T}\int_{t_o}^{t_o+T} x^2(t)\,dt}$.

(IV) Repeat the calculations of (III) but now use a 2V rms input sinusoid and assume a simple 0.7V model for the diode (V_D = 0.7 volts for forward current, I_D = 0 for reverse voltage). Also, use SPICE with a 5mA, n=1.5 diode model to simulate the output waveform for a 60Hz input frequency.

EXPERIMENT

(1) First, consider how we might use the oscilloscope to display the current vs. voltage characteristic for the junction diode. In order to do this we must be able to display the diode voltage, V, on the horizontal axis of the 'scope and the diode current, I, on the vertical axis. Thus, the 'scope should be set up in XY mode. The circuit in Figure 4.10 shows one way to display the diode current as a voltage on the 'scope screen.

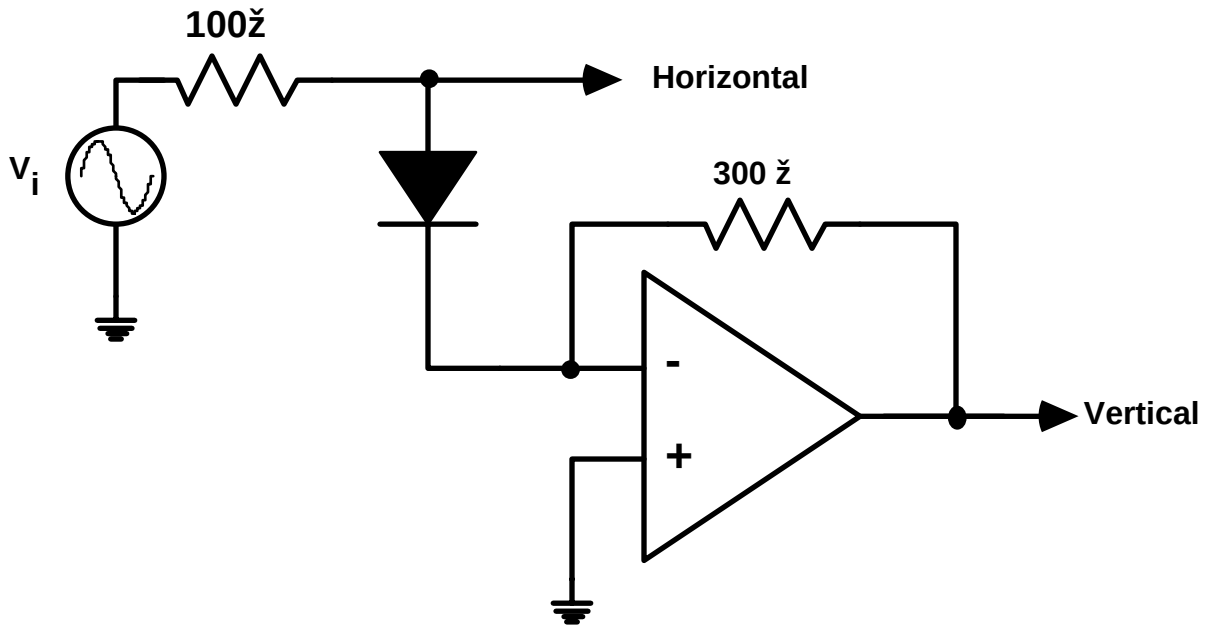


Figure 4.10

The operational amplifier forces the cathode of the diode to be held at approximately zero volts. Thus, the voltage measured at the anode of the diode is, in fact, the diode voltage, V_D. Noting that the diode current flows through the 300Ω feedback resistor, the op amp output voltage is given by $-300 \cdot I_D$. Thus, the output voltage of the op amp is directly proportional to the diode current, I_D. The oscilloscope can now be used to display the diode characteristic. *NOTE* that this technique is limited by the output current capability of the op amp, typically 25 - 50 mA.

Assemble the circuit of Figure 4.10 using the trainer breadboard. Carefully record the voltage and current measurements made from the 'scope screen, and also sketch the displayed diode characteristic. Can you think of any other way to use the 'scope to display the diode I vs. V curve?

Next, use the *curve tracer* instrument in the lab to produce the I vs. V curve for the diode. Obtain a printout of the results, if possible.

(2) Now carefully measure the diode voltage and current using the DMM with the circuit of Figure 4.11 over the range $-10 < V_{in} < +10$ volts. Make sufficient measurements to produce a reasonable plot of the characteristic to compare with the 'scope and curve tracer measurements. Use the measurements to deduce the value of I_s and the product nV_T. To avoid the complication of the internal resistance of the

multimeter in "current" mode, determine the diode current by measuring the voltage across the known resistor value and applying Ohm's law.

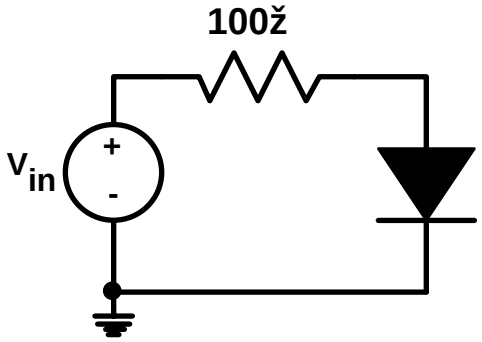


Figure 4.11

(3) Construct the *half-wave rectifier* circuit of Figure 4.6. Use the function generator for the signal source and R=680Ω. Adjust the function generator for a sinusoidal input signal at approximately 1kHz with 1 volt amplitude (2 volts peak-to-peak). Using the 'scope, measure the input and output voltage waveforms and the diode current and voltage waveforms (I_D and V_D). Record your measurements carefully by sketching and labeling the waveforms.

Now repeat the measurements with a sinusoidal input of 10 volts amplitude (20 V p-to-p).

Finally, repeat the measurements with a *square* wave input of 10 volts amplitude.

(4) Construct the *full-wave rectifier* circuit of Figure 4.7, using R=680Ω. Measure the input and output voltage waveforms by carefully sketching the oscilloscope display for: (i) 1kHz sinusoid with 2 volts amplitude, (ii) 1kHz sinusoid with 10 volts amplitude, and (iii) 1kHz square wave with 10 volts amplitude.

RESULTS

(a) Present your measurements from parts 1 and 2 of the experiment. Discuss the merits of the three techniques (oscilloscope, curve tracer, and DMM) used to measure the diode current vs. voltage characteristic. Which is easiest to do? Which yields the most precise results?

(b) Sketch the input and output voltage waveform measurements (sine wave and square wave) for the half-wave rectifier of part 3. Also sketch the diode voltage and current waveforms. Discuss the measurements.

From your measurements with a 10 volts sinusoid input, what is the voltage peak amplitude "loss" between the input and output waveforms due to the diode voltage drop (express your answer as a percentage)? What would you expect the percent loss be if the input were 120 volts rms?

Because the junction diode is not an ideal conductor in the forward direction, power is dissipated in the diode ($V_D \cdot I_D$). Determine the rms power dissipated in the diode for the 10 volt sinusoid input case. How does this compare to the rms power delivered to the load?

(c) Sketch the input and output voltage waveforms for the full-wave rectifier circuit of part 4. What is the maximum (peak) forward and reverse bias voltages for the bridge diodes with 20 volts peak-to-peak input? What is the rms current through each of the diodes in this case? Estimate the rms power dissipation in the diodes and the load.

(d) What additional concepts or measurements should be added to this experiment to make it better?

Revised 7/94

Lab # 5
TITLE: Nonlinear Circuit Applications: Diodes and Op Amps

ABSTRACT

Many important electrical applications involve *signal processing* to extract useful information about an input signal (peak value, RMS value, relative phase, amplitude envelope, etc.). Several nonlinear circuits involving diodes and operational amplifiers are designed and constructed in this experiment. The effects of including nonlinear elements in the feedback loop of an op amp is also examined.

INTRODUCTION AND THEORY

This experiment involves the construction and evaluation of several elementary nonlinear circuits. Actually, it is probably more accurate to say "deliberately nonlinear", since most electrical components are nonlinear to a greater or lesser degree. This experiment is intended to present several examples of simple signal processing circuits, and is certainly not an exhaustive treatment of nonlinear circuit applications.

Limiter and Clipper Circuits

The major characteristic of many nonlinear circuits is that the behavior of the circuit varies with the amplitude of the input signal. Consider the *limiter* circuit shown in Figure 5.1.

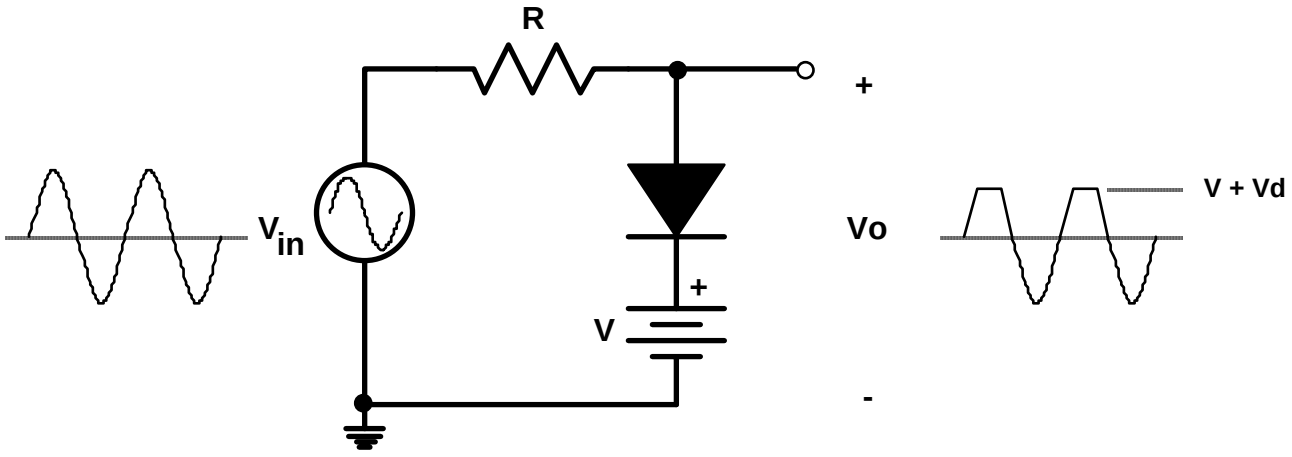


Figure 5.1

No current flows in the loop until V_{in} becomes great enough to turn the diode "on". If the diode is "off" (not conducting) there is no current through the loop, meaning that there is no voltage across the resistor (Ohm's law). This implies that *the output voltage, V_o, is equal to V_{in} as long as the diode is off*. When V_o becomes sufficiently high to start conduction through the diode ($V_o \approx V + V_{d(on)}$ volts), the output voltage gets *clamped* or *limited* to approximately V + 0.7 volts. If the input voltage goes higher, current flows through the loop, resulting in a voltage drop across the resistor. Note that if the input voltage never exceeds $V + V_{d(on)}$ then the output voltage is equal to the input voltage, while if V_{in} exceeds $V + V_{d(on)}$ then the output is clipped. A bipolar limiter (or *clipper*) can be constructed also, as shown in Figure 5.2.

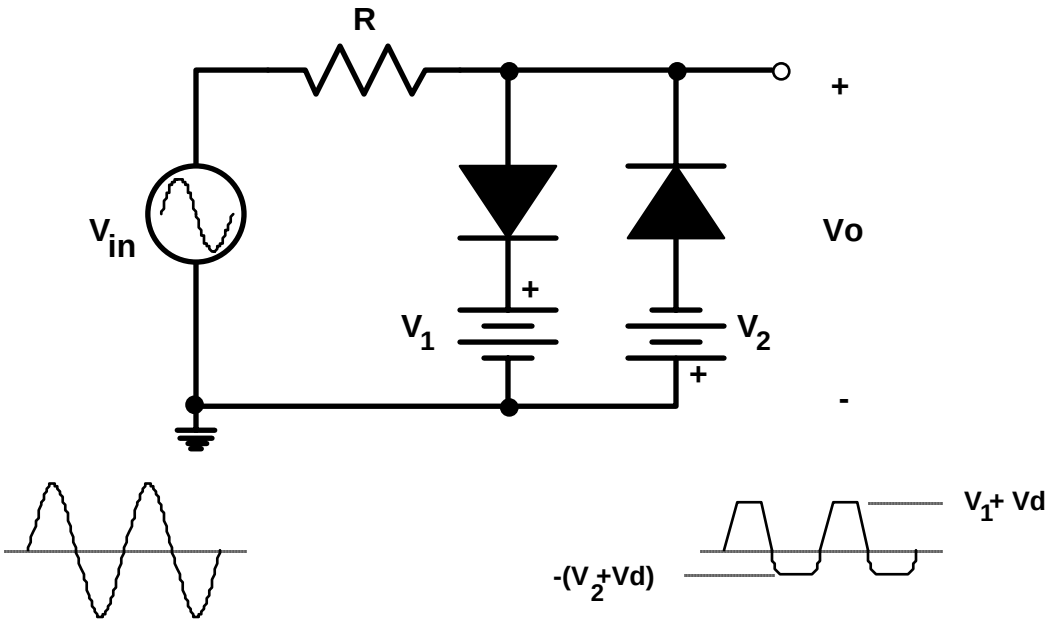


Figure 5.2

Precision Half-wave Rectifiers

There are situations in signal processing where we need to obtain a half-wave or full-wave rectified version of a signal with low amplitude. The simple rectifiers considered in the previous lab experiment have the drawback that there must be a voltage drop across the diode(s) in the rectifier circuit, causing the peak amplitude of the output voltage to be smaller than peak input amplitude. In a power circuit where the peak voltages are tens or hundreds of volts the loss of a volt due to the rectifier circuit is probably tolerable. However, this loss is often unacceptable if the input voltage is a few

volts or less: an input voltage in the millivolts range may not even turn on the simple diode rectifier.

One way to simulate an ideal diode characteristic in a low-power circuit is to employ an op amp. Consider the circuit of Figure 5.3, known in the vernacular as a *superdiode* circuit. In this circuit a real junction diode is connected in the feedback path of the op amp.

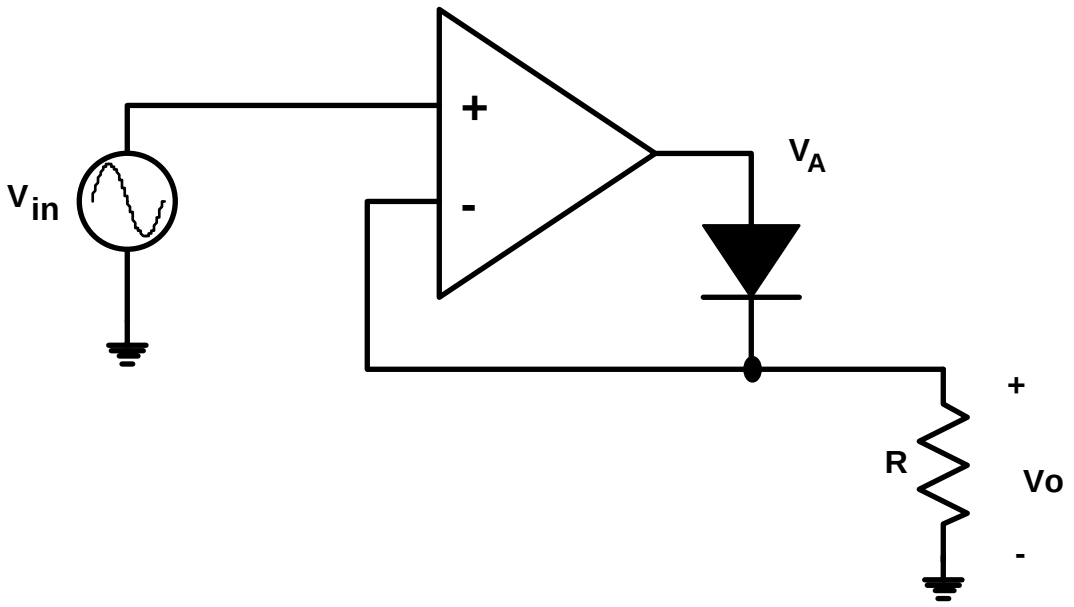


Figure 5.3

There are several important features to notice about this circuit:

- The only way for current to flow in the load resistor, R, is to have current flow through the diode (since the op amp input is presumably acting like an open circuit). This also means that V_o will only be positive since current flows through the diode in only one direction.

- If the diode is conducting, the op amp's negative feedback path is electrically connected: op amp output, through the diode, and back to the inverting input. This means that the op amp will attempt to force the voltage difference between its two inputs to be nearly zero (virtual short). With no voltage difference between the op amp inputs, *V_o must be equal to V_{in}* when the diode is conducting (forward bias).

- In order for the diode to conduct the voltage at the op amp output, V_A, must be greater than V_o by an amount equal to the required diode "on" voltage.

- If the diode is not conducting (reverse biased), the op amp's negative feedback path is *not* connected, meaning that the op amp output cannot affect the input. Under these conditions any voltage difference between the two op amp inputs results in a large voltage swing at the op amp output, since the input difference is multiplied by the large differential gain of the op amp. In a real op amp this usually means that the output will *saturate* at the limiting output voltages, V_{MAX} and V_{MIN}. *Note* that without the negative feedback path we *cannot* assume a virtual short circuit at the op amp inputs.

The behavior of the circuit is made more clear by considering a plot of V_o and V_A vs. V_{in} for the circuit, as shown in Figure 5.4.

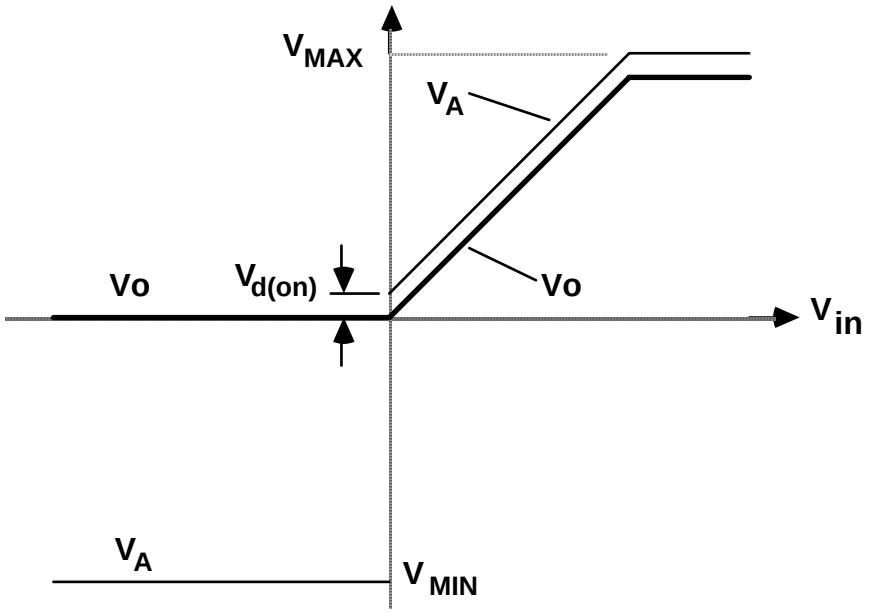


Figure 5.4

When V_{in} is greater than zero, the op amp output voltage, V_A, increases until the diode just turns on, thereby closing the negative feedback loop and forcing V_o to be equal to V_{in}. As long as $V_{in} > 0$, V_A stays approximately 0.7 volts above V_o. If V_{in} increases above the voltage range of the op amp output swing then the op amp saturates in the positive direction, as indicated in the figure.

When V_{in} is less than zero, the op amp output attempts to keep the voltage difference between the op amp inputs near zero by swinging in the negative direction. However, this reverse biases the diode, forcing V_o to zero and breaking the negative feedback path. Thus, V_A keeps swinging as negative as it can get: the negative saturation voltage.

The usable range of input frequencies for the superdiode is somewhat limited in practice because the voltage V_A must change abruptly from near V_{MIN} to $V_{d(on)}$ as the input voltage goes from negative to positive. Changing the op amp output from one voltage to another requires time because of the *slew rate* limitations of the op amp: only a finite amount of current is available to charge up the internal capacitance of the amp. Another problem with the superdiode circuit is that the differential input voltage ($v_+ - v_-$) is equal to $|V_{MIN}|$, which may exceed the input voltage specification of some op amp types.

A modified superdiode circuit that remedies some of the problems of the simple superdiode is shown in Figure 5.5.

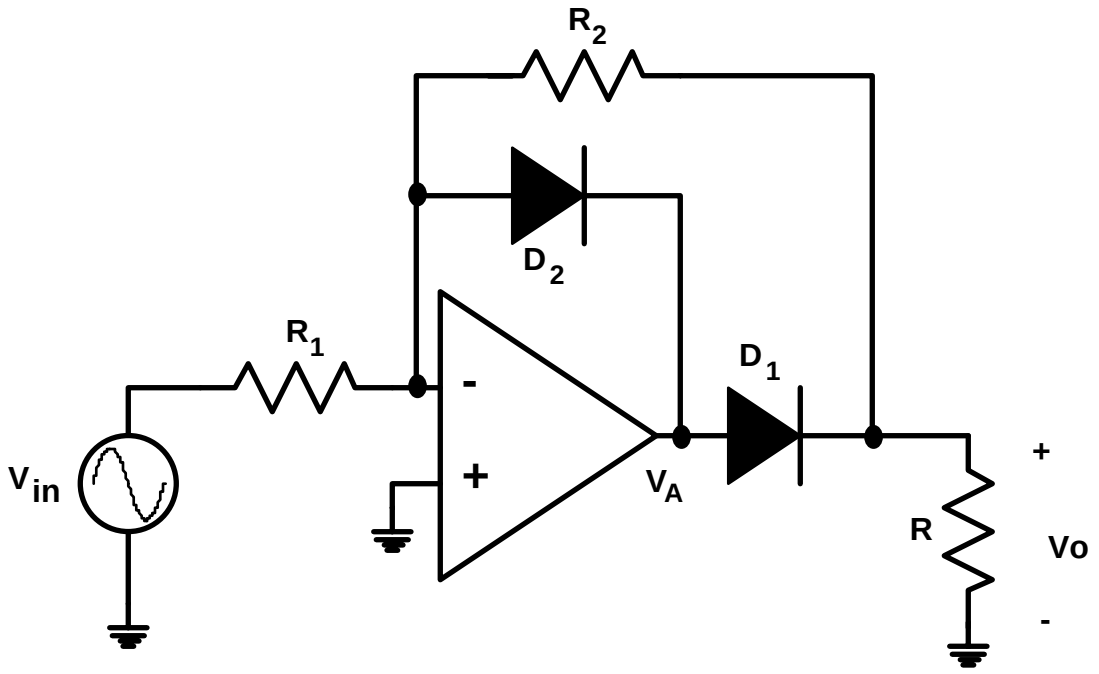


Figure 5.5

In this circuit a second diode has been added to prevent the op amp output from going all the way to V_{MIN} when the output diode is off. In other words, diode D_2 closes the

negative feedback path for positive V_{in}, and D_1 closes the negative feedback path for negative V_{in}. The result is that the op amp does not go into open loop saturation, which allows the circuit to operate with higher input frequencies. Furthermore, the action of D_2 to "catch" the op amp output before it saturates allows the amp to maintain a virtual ground at the inverting input and prevents the large differential input voltage found in the simple superdiode circuit. The transfer characteristic (V_o and V_A vs. V_{in}) is shown in Figure 5.6. Note that the circuit is an inverting half-wave rectifier, with gain adjustable by selecting the ratio of R_2/R_1.

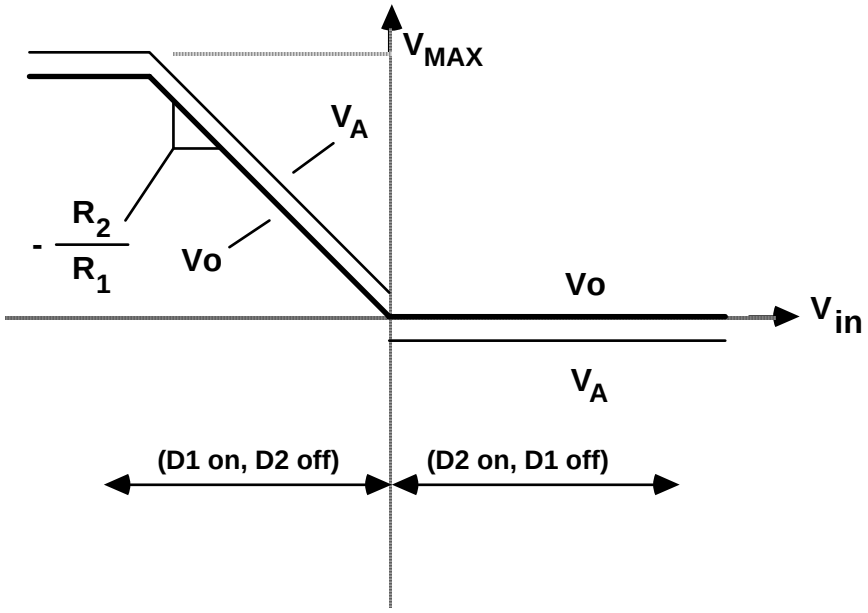


Figure 5.6

Peak Rectifiers for AC-to-DC conversion

A peak rectifier, or *peak detector*, is a circuit that acquires and "holds" the peak value of a time varying waveform. Peak rectifiers are used to produce a nearly constant DC voltage from an AC input waveform for use in DC power supplies. They are also used in *envelope detection* of waveforms, such as demodulation of amplitude modulation (AM) broadcast material.

Consider the circuit of Figure 5.7. If we neglect the forward voltage drop across the diode and assume that the capacitor is ideal it is apparent that current will flow through the diode and charge up the capacitor whenever V_{in} exceeds V_o.

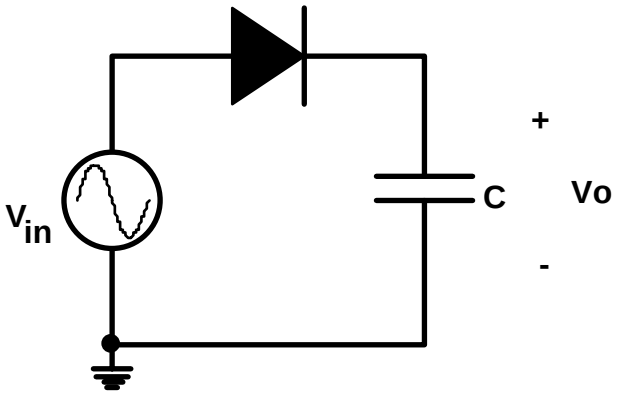


Figure 5.7

Moreover, once the charge is stored on the ideal capacitor it must stay there, since there is no current path in reverse through the diode to discharge it. V_o holds the peak value of V_{in}*. The peak rectifier circuit can be used to take an AC input voltage waveform and produce a DC output voltage, which is useful in DC power supply applications.

In a practical peak detector circuit there will always be some charge lost from the capacitor, either due to leakage in the capacitor package or due to additional circuitry attached as a load to the peak detector circuit. Thus, the capacitor voltage will tend to *droop* from its peak value. Consider the peak detector of Figure 5.8, where the leakage and loading have been modeled by a parallel resistance.

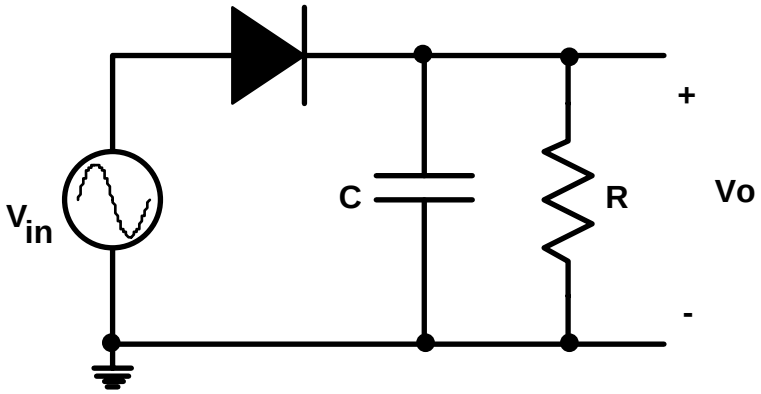


Figure 5.8

* Since a real junction diode will be used, however, V_o will be *less* than the peak value of V_{in} due to the forward voltage drop of the diode.

Once an input voltage peak has been passed and the diode shuts off, the voltage across the capacitor will drop exponentially from its peak value with the RC time constant of the circuit, namely $V_c(t) = V_{peak} \cdot e^{-t/RC}$. As shown in Figure 5.9 the droop results in an output voltage with *ripple*, rather than a constant value.

If we know that V_{ripple} is small compared to V_{peak} (the amplitude of the input voltage) then we can make the approximation that $T_{discharge}$ is approximately equal to the input waveform period, T. This approximation further implies that T/RC is much less than one, i.e., the discharge time constant is long compared to the period of the input sinusoid. Applying this approximation:

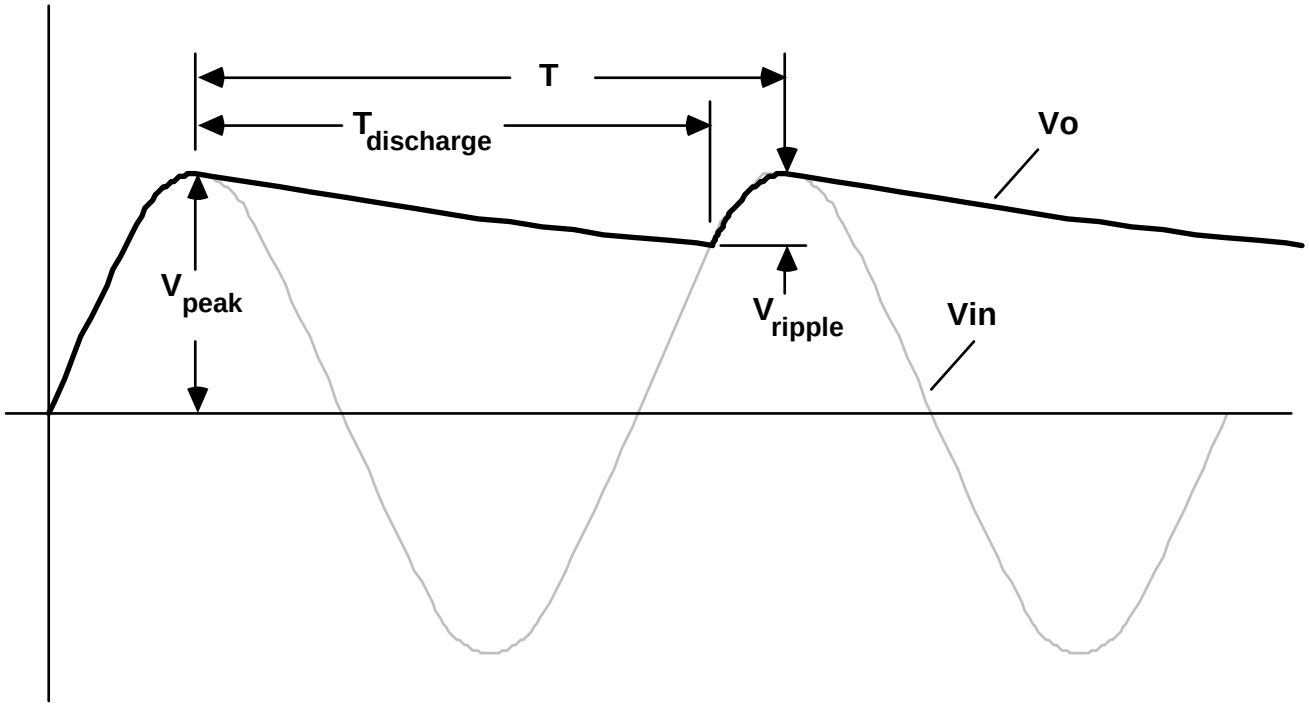


Figure 5.9

$$V_c\left(T_{discharge}\right) \approx V_c(T) = V_{peak} \cdot e^{-T/RC}$$

and

$$V_{ripple} \approx V_{peak}\left(1 - e^{-T/RC}\right).$$

Since the exponent T/RC << 1, this last expression can be simplified further using the approximation $e^x \approx 1 + x$ for x << 1, yielding

$$V_{ripple} \approx V_{peak}\left(1 - \left(1 - \frac{T}{RC}\right)\right)$$

$$\approx \frac{V_{peak} T}{RC} = \frac{V_{peak}}{fRC} \quad ,$$

where *f* is the frequency of the input sinusoid.

We can design the circuit to reduce the ripple by either increasing the frequency of the input signal (shortening the discharge *period*) or increasing the RC time constant (lowering the discharge *rate*). In a practical power supply design situation we usually cannot do much about the current supplied to the load ($I_{load} = V_c(t)/R_{load} \approx V_{peak}/R_{load}$), since this is usually fixed by the requirements of the circuit to be powered by the supply. Similarly, the input frequency cannot usually be altered if a 60Hz power line signal is used, although a *full-wave rectifier* is typically employed to double the effective operating frequency (see Lab #4). This leaves the size of the capacitor as the major design choice.

Voltage Conversion: the Voltage Doubler

The simple peak rectifier can be altered to produce a DC output voltage approximately equal to the *peak-to-peak* value of the input signal. This *voltage doubler* circuit is shown in Figure 5.10.

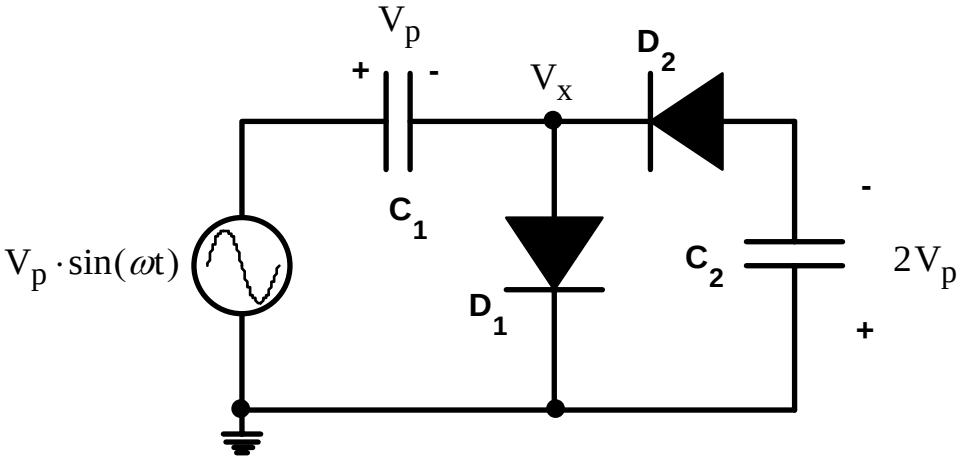


Figure 5.10

The circuit operates as follows. When the input signal is positive, current is induced to flow through capacitor C_1, through diode D_1 in the forward direction, and back to the source. D_2 is reverse biased under these conditions, and the voltage V_x is equal to the diode "on" voltage of D_1. This charges C_1 to approximately the peak voltage of the input waveform, V_p (neglecting the diode voltage drop).

When the input signal decreases from its peak value the voltage at V_x is forced negative due to the stored DC voltage ($\sim V_p$) across C_1. This causes current to flow through capacitor C_2, through D_2 in the forward direction, and tends to discharge C_1. After several cycles of the input waveform the two capacitors approach the DC voltage values indicated in Figure 5.10. At the negative peak of the input signal the voltage at V_x is approximately $-2V_p$: V_p from the input and an additional $-V_p$ due to the stored voltage across C_1. This charges C_2 to approximately twice the peak value of the input waveform, hence the voltage "doubler" name of the circuit. Note that the voltage across C_2 will exhibit the same droop characteristics as the basic peak rectifier circuit if any load is connected to the circuit.

Precision Peak Detection

A different consideration regarding peak rectifiers is the design of so-called *precision* peak detectors suitable for low power (i.e., op amp level) signal detection applications. The circuit of Figure 5.12 shows a precision peak rectifier using a superdiode circuit. This circuit reduces the effect of the diode's forward voltage in the basic peak rectifier of Figure 5.7, but droop due to loading will still be present.

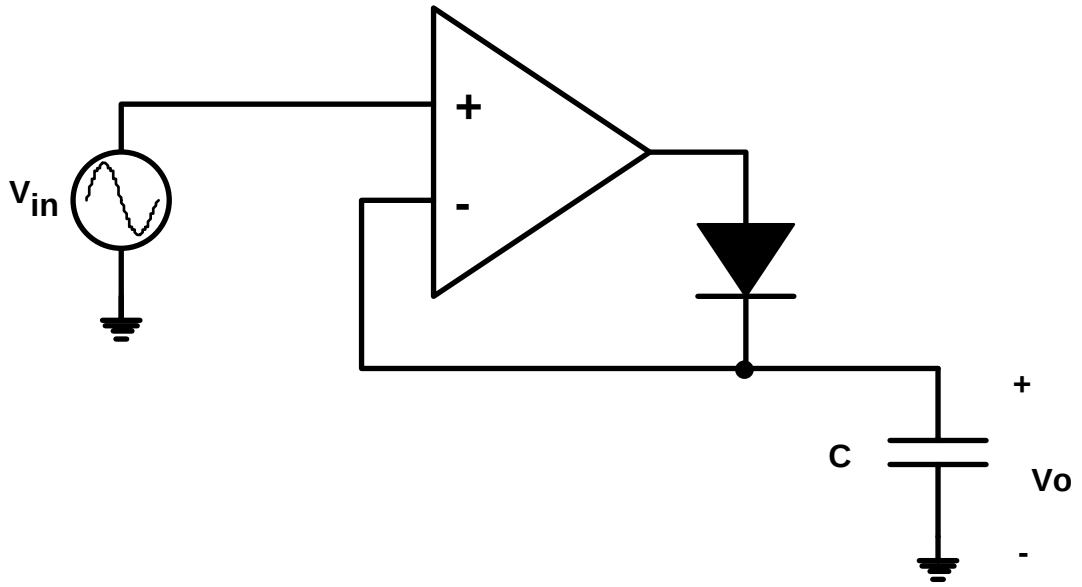


Figure 5.12

A more refined peak detector is the *buffered precision peak rectifier* shown in Figure 5.13. In this circuit the voltage across the capacitor is buffered by op amp A2 (A2 should be a low input current device), which reduces voltage droop by isolating the charge storage capacitor from any attached load circuitry. The circuit also has a negative feedback path around the entire circuit, forcing the output voltage to equal the applied peak input voltage. Circuits of this type are useful when a peak voltage is to be held for a relatively long period of time. Some designs include a switch in parallel with the charge storage capacitor in order to reset the held voltage to zero.

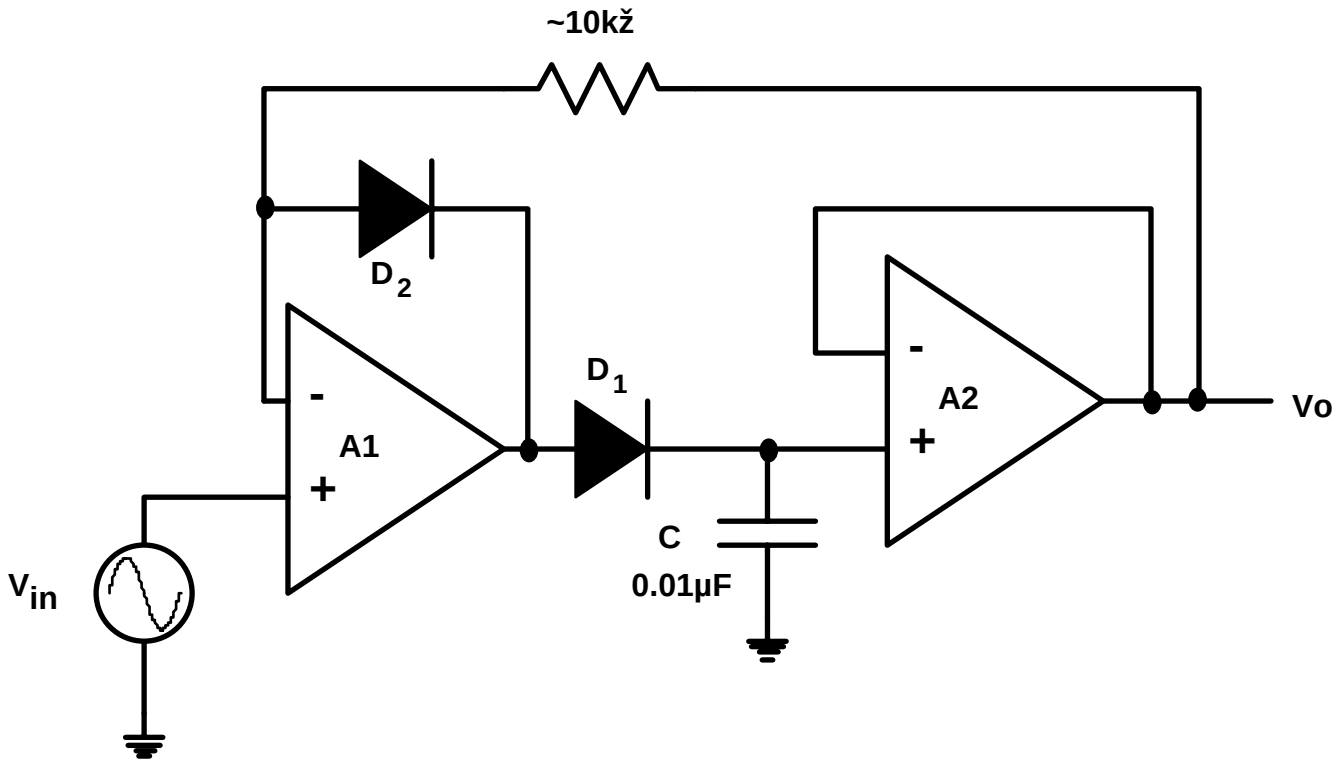


Figure 5.13

Comparators and Bistable Multivibrators

There are many signal processing tasks where it is necessary to compare two voltages and determine which one is greater. A circuit that performs this function is called a *comparator*. The common circuit symbol for a comparator looks like the symbol for an op amp–and, in fact, an op amp is often used for this purpose. The open loop differential gain, A, of the op amp results in an output given by $V_{out} = A(V_+ - V_-)$. With no negative feedback the op amp output will be constrained by the power supply voltages to either be the maximum positive value ($V_+ > V_-$) or the maximum negative value ($V_+ < V_-$).

Consider the lightbeam-activated door-opener system depicted in Figure 5.14. The photo cell has a small electrical resistance when exposed to the light beam, and a large resistance when the light beam is interrupted. The comparator circuit produces a *high* output voltage ("open the door") when the beam is interrupted and a *low* output voltage when the beam is striking the sensor ("let the door close").

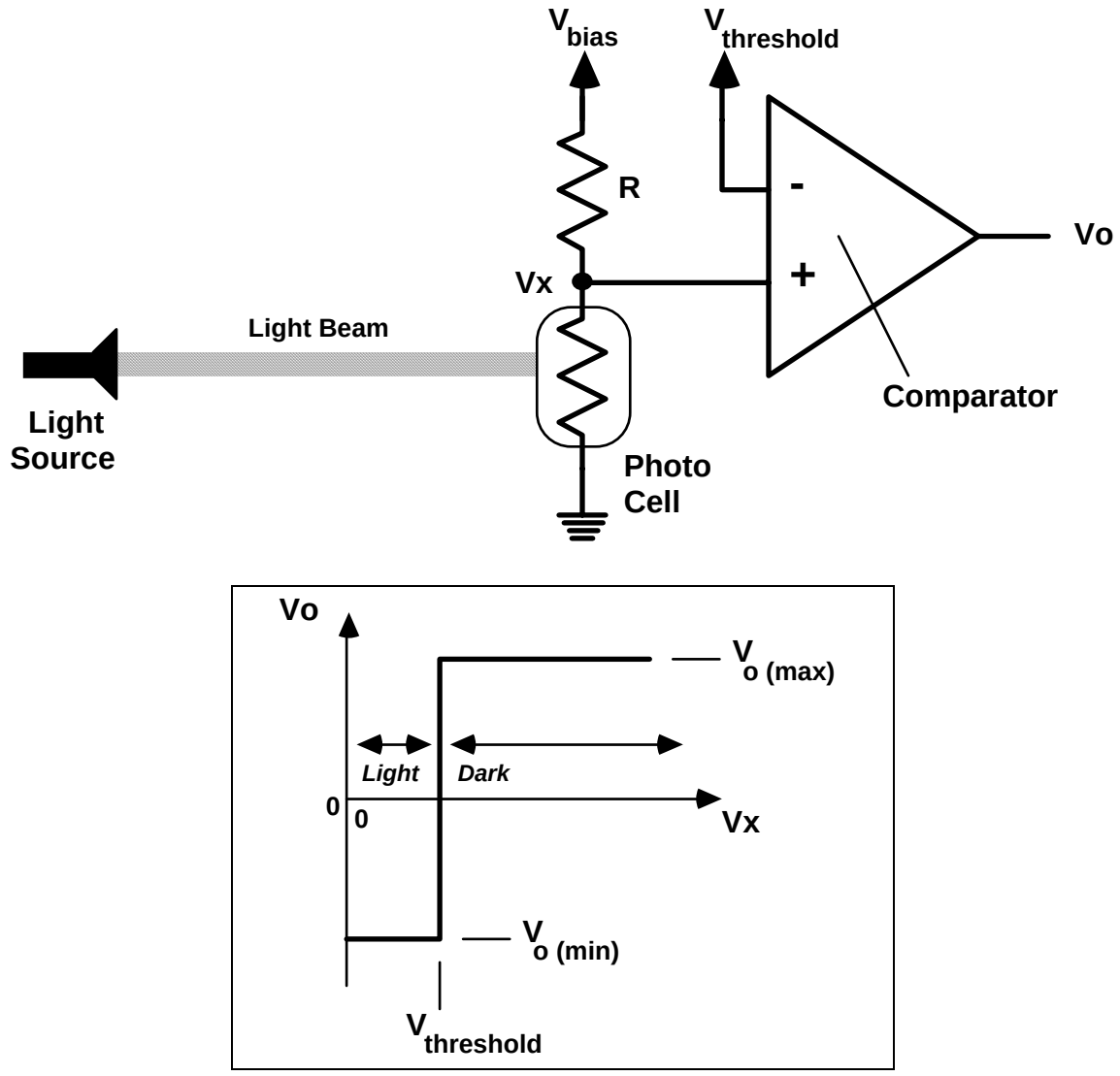


Figure 5.14

The voltage V_x is determined by the voltage division relationship between the photo cell resistance, R_{cell}, and the fixed resistance, R:

$$V_x = V_{bias} \cdot \frac{R_{cell}}{R + R_{cell}}$$

The *threshold* voltage ($V_{threshold}$) is selected so that $V_x < V_{threshold}$ when the light beam is striking the photo cell (R_{cell} is small), and so that $V_x > V_{threshold}$ when the beam is interrupted (R_{cell} is large).

The circuit of Figure 5.14 can be modified for other purposes, such as a thermostat control that would start and stop a furnace using a temperature sensor instead of a light beam and photo cell. One problem with the circuit, however, is that any electrical *noise* that might be present in V_x can result in the input to the comparator fluctuating above and below the threshold voltage, causing the output to change state rapidly between high and low. This is due to the fact that the high-to-low and low-to-high transitions occur at the same input voltage.

A comparator circuit that avoids this problem is shown in Figure 5.15. *Note* that the circuit uses positive feedback instead of the negative feedback you have encountered before.

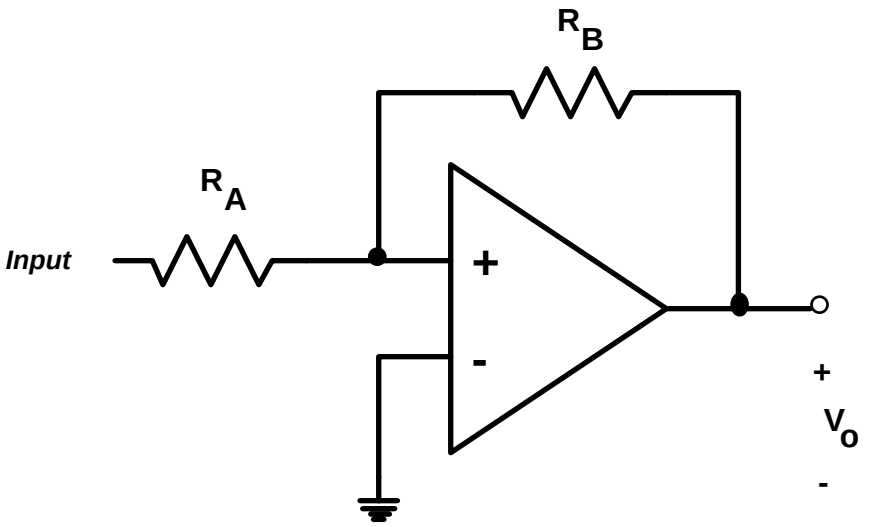


Figure 5.15

The positive feedback causes the circuit to be *unstable*, forcing the output voltage to be pegged at its maximum positive or minimum negative value. This is because even with the output near zero, just a miniscule voltage difference between the op amp inputs will cause the output to start swinging higher or lower. In either case the output affects the input through the positive feedback resistor, causing the output to swing farther in the *same* direction until reaching the positive or negative output extremum. It is important to remember that the "virtual short circuit" concept describing the two op amp inputs applies only for linear, negative feedback operation. This means that the positive feedback circuit of Figure 5.15 *cannot* be analyzed by assuming a virtual ground at the non-inverting input.

If the voltage at the noninverting op amp input is *greater* than the voltage at the inverting input (grounded) then the output will be $V_{o(max)}$, while if the voltage at the noninverting input is *less* than zero then the output will be $V_{o(min)}$. Since the output transition occurs when the noninverting input is at zero volts, an interesting feature of this circuit is that the input threshold voltage for the comparator is derived from the output voltage and the voltage divider of the resistors in the feedback network. In other words, the threshold voltage will be different depending upon whether the present output voltage is positive or negative. This characteristic, shown in Figure 5.16, is known as *hysteresis*. In practice, the width of the *hysteresis loop* is chosen large enough to reduce the effects of any noise or interference riding on the input signal, but small enough to retain the required comparator action.

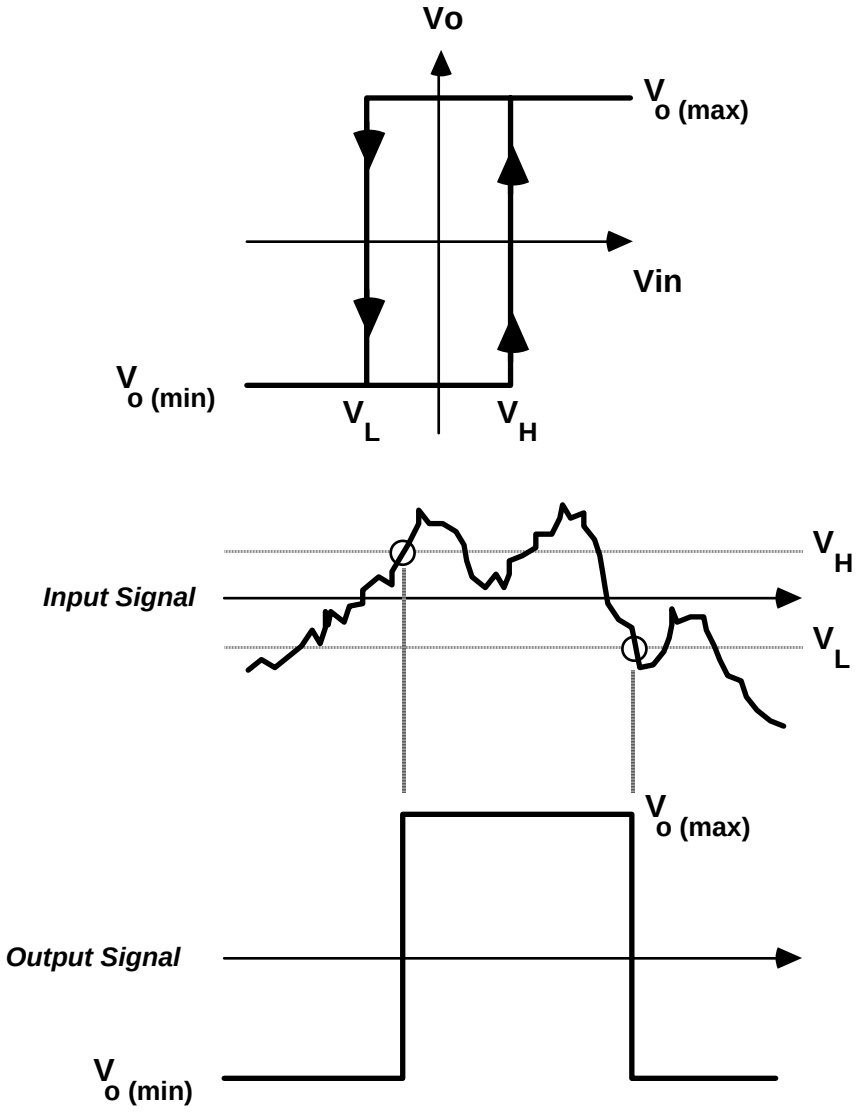


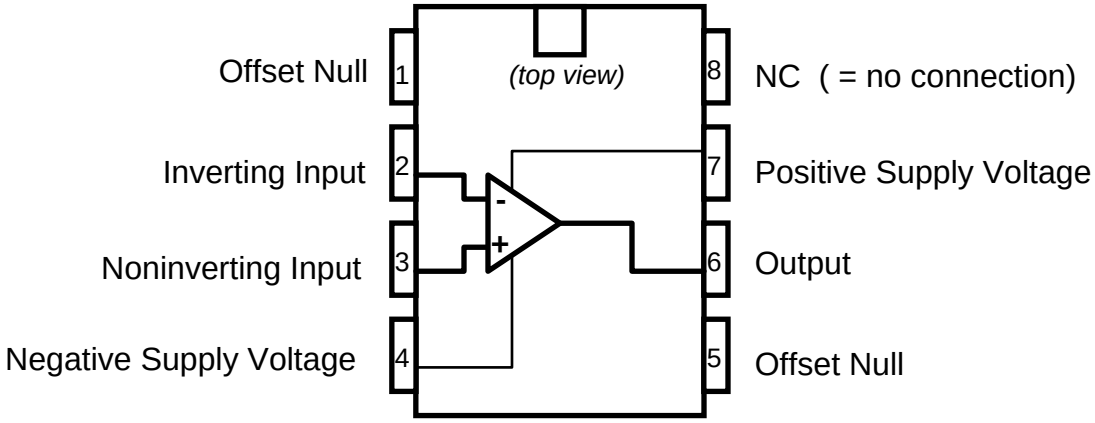
Figure 5.16

REFERENCES

See Chapter 3 and Chapter 12 of the text by Sedra and Smith, *Microelectronic Circuits*, 3rd ed., Saunders College Publishing (Holt, Rinehart, and Winston), 1991.

EQUIPMENT

Lab component kit (resistors, op amp, and diodes) Power supply
Digital Multimeter (DMM) Function generator Oscilloscope
Heathkit trainer



Type 741 op amp pinout

PRE-LAB PREPARATION

(I) *Using the diode equation*, solve for the diode current and output voltage in the circuit of Figure 5.17 with (a) V_{in} = 5 volts, and (b) V_{in} = 10 volts.

Assume that the diode has n=2, and is known to conduct 10mA when V_d=0.7 volts, i.e., a "10mA diode".

(II) Consider the superdiode circuit of Figure 5.3. Using the `ua741` op amp model, a 1mA diode with n=2, and R=2.2kΩ, use PSPICE to generate a plot of V_o and V_A for -15 ≤ V_{in} ≤ +15 volts. Use ±15 volt supplies for the op amp. Explain the results.

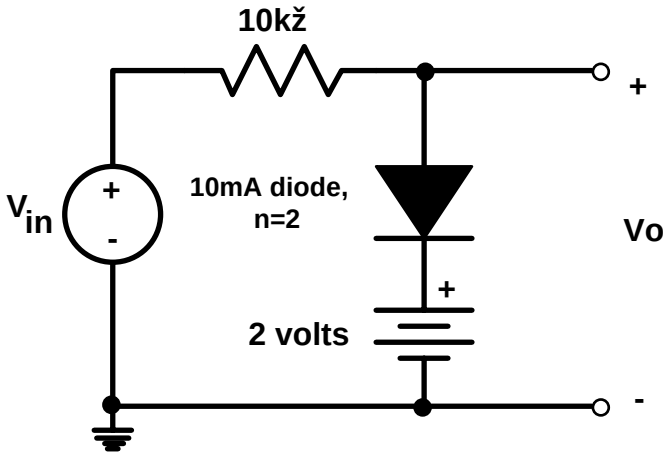


Figure 5.17

(III) Assuming an ideal diode in the circuit of Figure 5.8 (i.e., short circuit when conducting in the forward direction), determine the amplitude of the output ripple voltage with R=220kΩ, C=0.1μF, and a 10 volt peak 60Hz sinusoidal input voltage. Use an "exact" calculation of the intersection of the exponentially decaying output voltage and the sinusoidal input voltage, and compare your result to the approximation from the introduction: $V_{ripple}=V_{peak}/fRC$. How do the calculations compare?

(IV) A hysteresis comparator (Figure 5.15) is to be designed with a symmetrical hysteresis loop 1.8 volts wide (transitions at V_{in} = -0.9 and +0.9). If the maximum output voltage of the op amp is ±12 volts and R_A=6.8kΩ, choose R_B to achieve the required hysteresis characteristic.

> *Hint*: note that as the input voltage increases from very negative voltages, the output is $V_{o(min)}$ and the voltage at the noninverting op amp input is determined by the voltage divider relationship among V_{in}, $V_{o(min)}$, R_A and R_B, namely
>
> $$V_+ = V_{o(min)} + (V_{in} - V_{o(min)}) \cdot R_B/(R_A+R_B).$$
>
> The transition from output "low" to output "high" occurs when the voltage at the noninverting input (V_+) reaches zero and starts to go positive. A similar situation applies for input voltages decreasing from very positive values.

EXPERIMENT

Note: Choose 2 out of the 4 parts of this experiment to perform for your report. Then, if you have time, feel free to try out some of the other circuits from the lab introduction: observe the behavior of the circuit, try some different component values, etc.

(1) Investigate the behavior of the simple limiter circuit of Figure 5.1 Using a DC power supply for V_{in}, R = 10kΩ and V = 2 volts, carefully measure and plot V_o vs. V_{in} for $-8 \le V_{in} \le +8$ volts.

Next, use the function generator for V_{in} and sketch the input and output voltage waveforms for several input waveforms, frequencies, and amplitudes.

What happens when you reverse the direction of the diode?

(2) Assemble and evaluate the superdiode circuit of Figure 5.3. Use a 741-type op amp and a 2.2kΩ load resistor. Sketch the V_o and V_A vs. V_{in} characteristic (DC) and the output waveform for input sinusoids of various frequencies and amplitudes. Determine the range of frequencies over which the superdiode circuit operates without noticeable distortion.

What happens when you reverse the direction of the diode?

(3) Examine the characteristics of the peak rectifier circuit shown in Figure 5.8. Assemble the circuit with C=0.1μF and a 10 volt peak 60 Hz sinusoidal input voltage, and sketch the input and output waveforms using the oscilloscope for several values of R. Make sufficient measurements to draw some conclusions about the behavior of the circuit. Also make some measurements and waveform sketches for several input frequencies greater than 60 Hz.

(4) Put together the hysteresis comparator designed in section (IV) of the pre-lab. Connect the function generator (~20 Hz) to the input and connect the oscilloscope in x-y mode so that the hysteresis characteristic is displayed on the 'scope screen. Sketch the V_o vs. V_{in} characteristic. Also observe and sketch the behavior of the comparator as the input frequency is increased.

Next, connect the input resistor R_A to ground, and move the input signal to the inverting op amp input, as shown in Figure 5.18. Observe and sketch the behavior of the circuit.

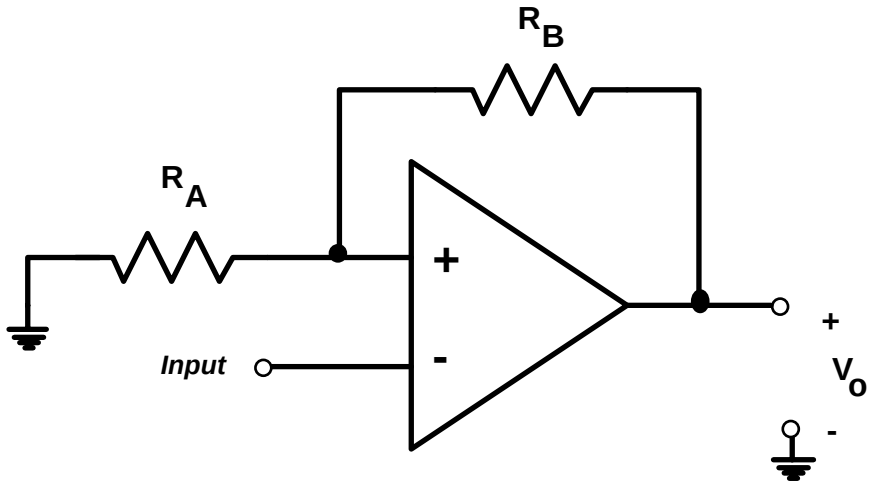


Figure 5.18

RESULTS

(a) Using your measurements from part 1, prepare a plot showing the DC output voltage and diode current as a function of the input voltage. Describe your measurements of the waveform "clipping action" of the circuit.

(b) Describe your measurements and evaluation of the superdiode circuit from part 2. Compare the DC measurements to the SPICE simulation from the pre-lab. What is the useful frequency and amplitude range for this circuit?

(c) Compare your results from part 3 with your expectations. How does the measured peak and ripple voltages compare to the approximations described in the lab introduction? What effect does the oscilloscope have on the measurements?

(d) Show your measurements of the hysteresis circuit. How do the results compare to the predictions from the pre-lab? Can you explain any differences? How did the operation of the circuit change when R_A was grounded and the input signal was applied to the inverting input?

(e) Describe any other circuits you examined in the lab.

(f) What would you add or remove from this experiment to make it better?

Revised 8/93

Lab # 6
TITLE: Bipolar Junction Transistors

ABSTRACT

The large-signal and small-signal terminal characteristics of the Bipolar Junction Transistor (BJT) are investigated in this experiment. BJT *models* are used to assist with the analysis and design of simple amplifier circuits. The behavior of a BJT in a current-booster circuit configuration is also considered.

INTRODUCTION AND THEORY

The bipolar junction transistor is a three-terminal device in which the voltage between (or current through) two of the terminals controls the current flowing in the third terminal. This means that the BJT can be used as a voltage controlled current source, which is useful in both the design of signal amplifiers and the design of solid-state electronic switches for digital circuits. The material in this introduction is only intended to be a summary of BJT concepts. Be sure to refer to your EEngr 360 textbook for a more careful treatment.

BJTs are physically composed of two back-to-back *pn* junctions (recall that a diode is simply a single *pn* junction). Two types of BJTs, the *pnp* and the *npn*, can be constructed. The circuit symbols for the devices are shown in Figure 6.1.

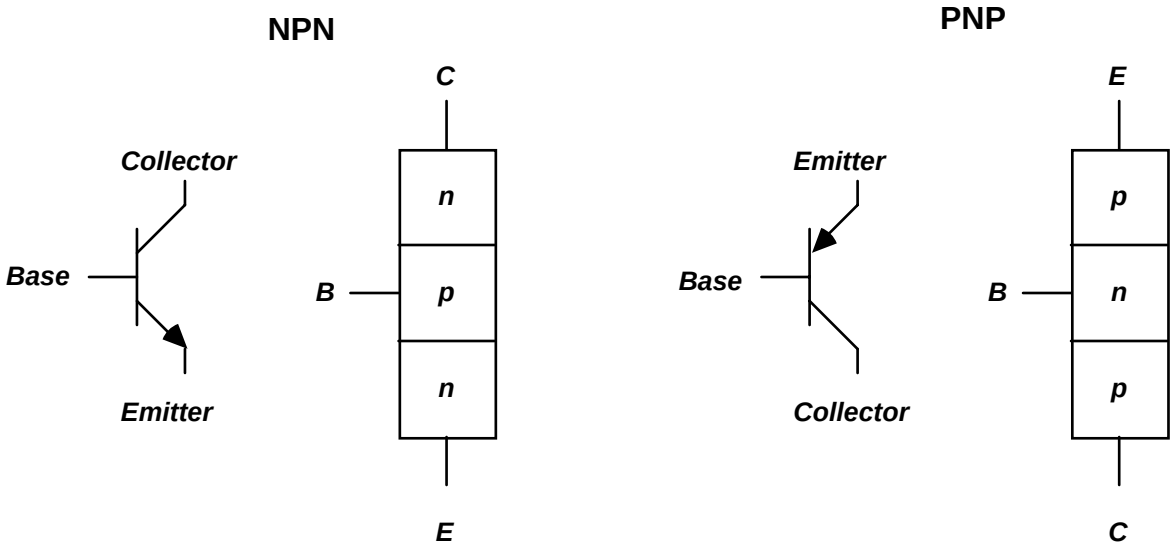


Figure 6.1

The arrow symbol is placed on the emitter terminal and points *out* for the NPN device and *in* for the PNP. You can keep track of the correct direction by remembering that the arrow points in the *forward* direction for the base-emitter junction, just like for a diode (from *p* to *n* type material).

The mode of operation for a BJT is determined by the external circuitry attached to the base, collector, and emitter terminals. In the *cutoff* mode both the base-emitter and the base-collector junctions are *reverse biased*, and no current flows through the device. The *saturation* mode, on the other hand, occurs when both junctions are *forward biased*, and current flows into the base and out the collector and emitter (NPN), or into the collector and emitter and out the base (PNP). Finally, the *active* mode of operation occurs when the base-emitter junction is *forward biased* and the base-collector junction is *reverse biased*. In the active mode the transistor behaves like a voltage controlled current source: current is actually induced to flow across the reverse biased base-collector junction under the control of the current across the forward biased base-emitter junction.

Active Mode BJT Characteristics

When operating in the active mode the operation of the BJT can be described with a set of equations relating the junction voltages and terminal currents. The normal current directions for active mode operation are shown in Figure 6.2. Note that the NPN and PNP devices operate in complementary fashion (current directions are reversed), but the active mode emitter current flows in the direction of the emitter arrow for both types of devices (out for NPN, in for PNP).

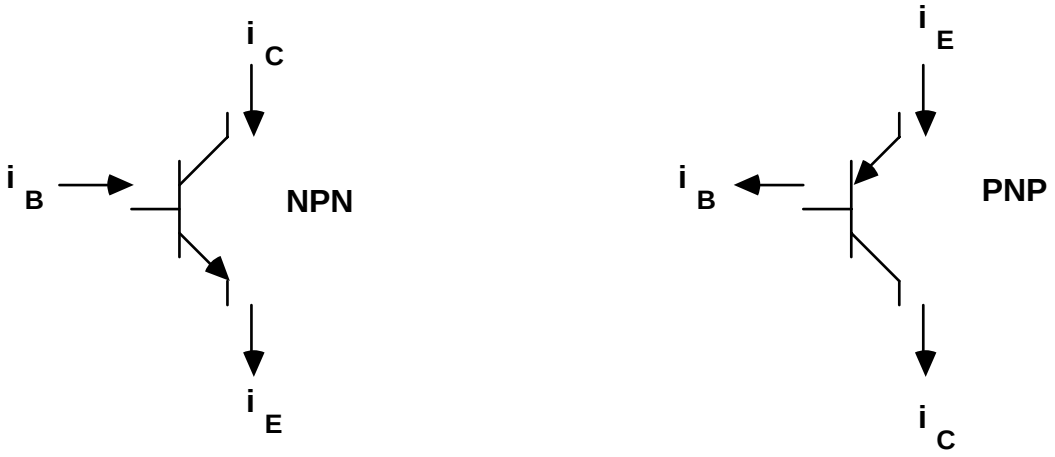


Figure 6.2

It is conventional to represent junction voltages and terminal currents using ordered subscripts. For example, the voltage across the base-emitter junction is indicated by v_{BE} and the base current by i_B. Note that $v_{BE}>0$ for an NPN device in the active mode, but $v_{EB}>0$ ($v_{BE}<0$) for an active mode PNP device. This can lead to some confusion at first about what symbols and polarities should be used in mathematical expressions. *Because the NPN and PNP devices are complementary, it is probably easiest to memorize the normal active mode current directions and junction biases for both types of devices, then choose the correct polarity in the equations*. In other words, an equation involving v_{BE} for an active mode NPN device becomes v_{EB} for an active mode PNP device. In practice, NPN devices are employed whenever possible because they operate at higher frequencies than similar PNP devices. This is because the current transported across the base of the transistor is primarily *electrons* in the NPN devices, but *holes* in the PNP device. The *mobility* of electrons is generally greater than the mobility of holes (nearly a factor of three in silicon), hence the faster operation of NPN devices.

The basic relationships to keep in mind are:

$$i_E = i_B + i_C$$

$$i_E = I_x e^{v_{BE}/V_T}$$

$$i_C = I_s e^{v_{BE}/V_T}$$, where V_T is the thermal voltage, kT/q.

The first equation ($i_E = i_B + i_C$) is simply KCL for the transistor: in steady-state conditions any current entering the BJT must equal the current leaving the device. The second equation is simply the diode equation for the base-emitter *pn* junction, with I_x representing the scale current. The third equation looks like the simple diode equation, but note that the current involved is i_C, while the junction voltage is v_{BE}! This is the essence of *transistor action*.

Since i_E and i_C both depend upon v_{BE} we can see that at a constant temperature:

$$\frac{i_C}{i_E} = \frac{I_s}{I_x} = \text{constant} = \alpha$$,

and since $i_E>i_C$, it is apparent that α is a number less than one ($0<\alpha<1$). Now, using the relationships $i_E = i_C/\alpha$ and $i_E = i_B + i_C$, we have:

$$\frac{i_C}{\alpha} - i_C = i_B$$

and

$$i_C = \frac{\alpha}{(1-\alpha)} i_B = \beta i_B .$$

This gives the additional active mode characteristics:

$$\beta = \frac{\alpha}{(1-\alpha)}$$

$$\alpha = \frac{\beta}{(\beta+1)}$$

$$i_C = \beta i_B$$

$$i_E = (\beta+1) i_B .$$

The parameter β (beta) represents the *current gain* of the BJT, and is often assumed to be a constant for a given device. Most transistors for use in signal amplifiers have betas somewhere in the range of 80 to 100, but "super-beta" transistors approaching 1,000 are also available. Large betas are desirable for signal amplifiers. Note that the parameter α is a number less than but nearly equal to unity for large values of β, since α=β/(β+1).

For the remainder of this experiment we will be concentrating on the use of NPN BJTs instead of PNP devices. This choice is primarily for convenience and brevity: PNP devices can be analyzed using the same procedure as NPN devices as long as the correct directions of the terminal currents are observed. *Do not* assume that PNP devices are somehow more difficult to use!

The various terminal characteristics for the BJT can be summarized in graphical form, as shown in Figure 6.3a and b. Figure 6.3a depicts the exponential relationship between the collector current, i_C, and the base-emitter voltage, v_{BE}.

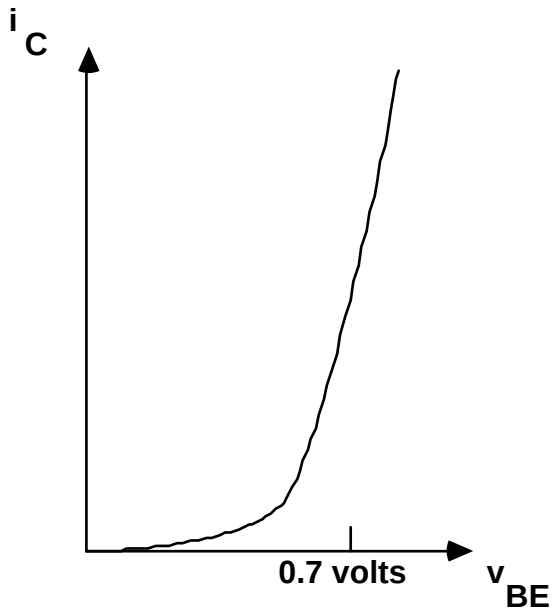


Figure 6.3a

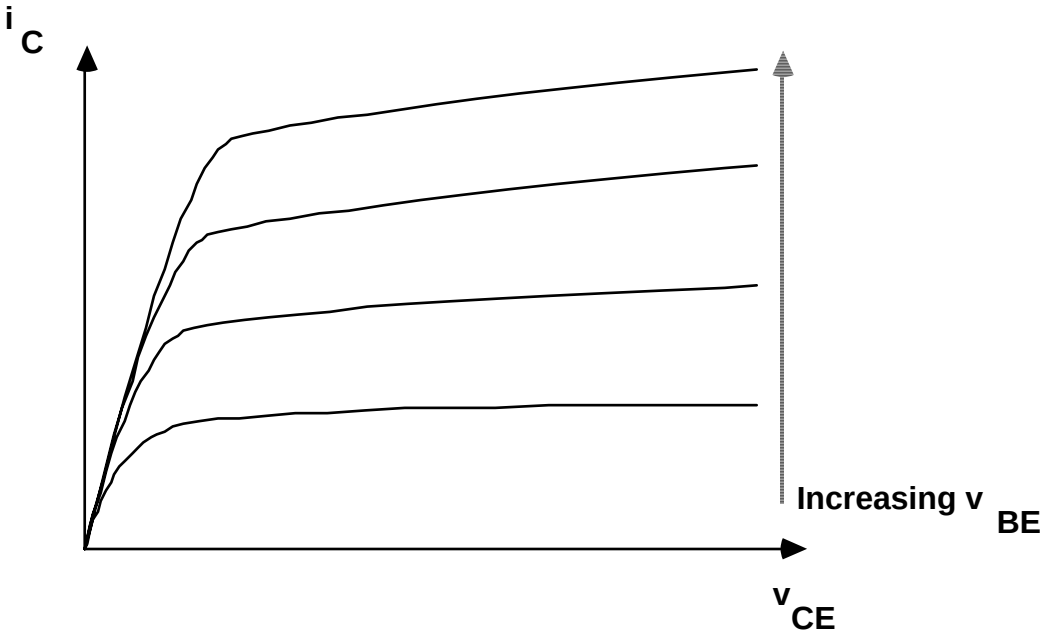


Figure 6.3b

Figure 6.3b shows the relationship between i_C and v_{CE} for several values of v_{BE}. For small values of v_{CE} the collector current decreases sharply as v_{CE} decreases, corresponding to the saturation mode of operation. Note that if v_{BE} is fixed, i_C remains relatively constant (horizontal) for a range of values of v_{CE}: this is the active mode

region of operation for the transistor. In this region the collector acts like a current source, remaining approximately constant as the collector voltage varies. Of course, the exact details of these curves varies from one BJT part number to another.

Recalling that an ideal current source would have an infinite output impedance, the non-zero slope of the i_C vs. v_{CE} curves in the active region is due to the *non-infinite output resistance* of the BJT (at the collector). One way that this effect is described for a BJT is in terms of the *Early voltage*[*] , V_A, which is the x-intercept of the extrapolated i_C vs. v_{CE} segments, as depicted in Figure 6.3c. Note that although the x-intercept is a negative value of v_{CE}, V_A is specified as a *positive* number. The greater the value of V_A, the flatter the i_C curves and the more ideal the BJT's current source behavior. A good BJT has $V_A > 50$ volts.

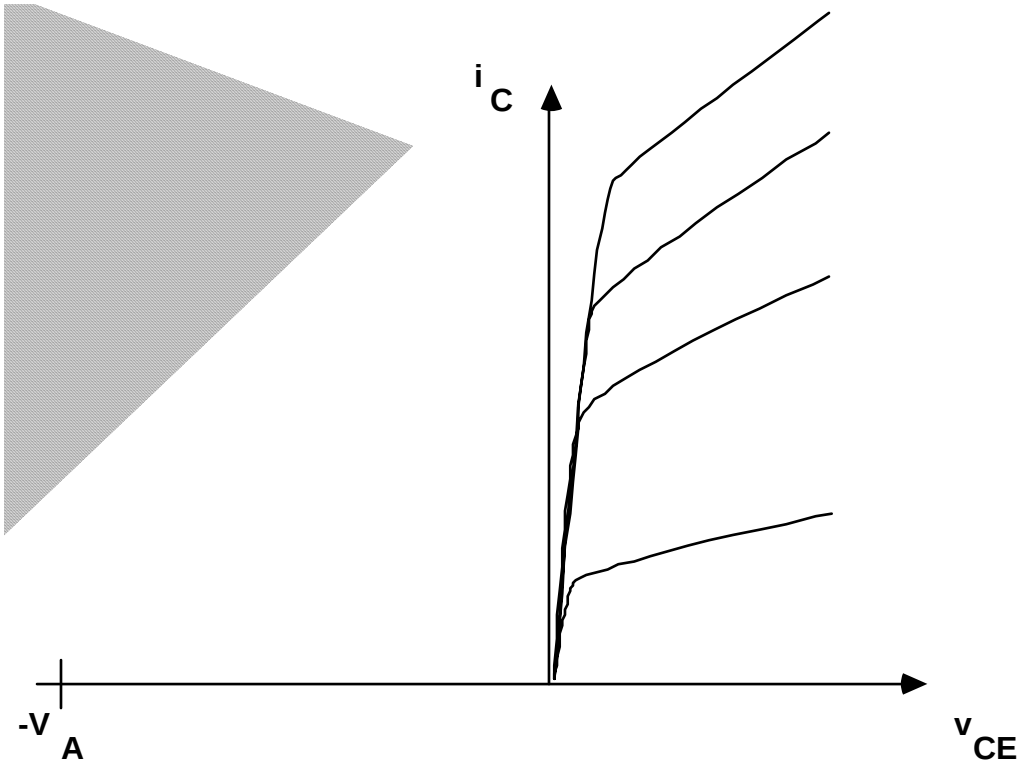


Figure 6.3c

Biasing and Small-Signal Approximations

[*] Named for J. M. Early, a semiconductor researcher.

A usable amplifier must have a *linear* input-to-output relationship so that the input signal is reproduced without distortion. Thus, in order to use a BJT as a signal amplifier we must deal with the *exponential* relationships between the junction voltages and terminal currents. Furthermore, a good amplifier design should be reasonably independent of the exact device parameters, such as β, since there is often a wide variation from transistor to transistor even with the identical part number.

The primary approach for linearizing a BJT is to add a DC *bias* voltage to a "small" amplitude AC input signal. The small AC input signal is the signal we want to amplify, and the DC bias voltage is added to help linearize the BJT. *As long as the amplitude of the input signal is kept sufficiently small, the sum of the bias voltage and the small input signal allows us to use a portion of the exponential curve as an approximately linear segment, while avoiding the decidedly nonlinear regions of operation*. Various methods are available to bias BJTs, and we will look at a few in this experiment.

Consider the circuit of Figure 6.4 below. The circuit is an example of a *common-emitter* amplifier, because the emitter of the NPN BJT is connected to the ground reference node. The input voltage (small amplitude signal plus DC bias) is applied at the base of the transistor and the output voltage is measured from the collector.

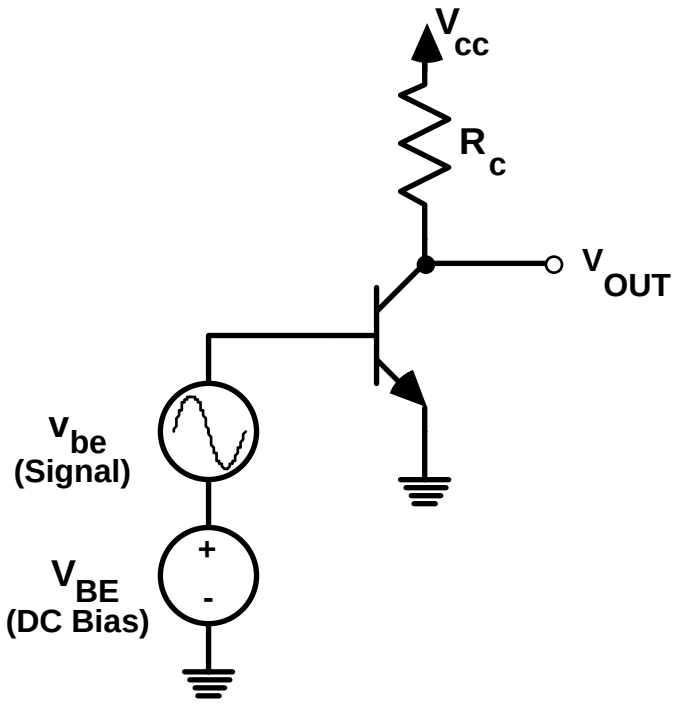


Figure 6.4

We can analyze this circuit mathematically for the active mode using the equations presented before. Since it is necessary to keep track of the DC input bias voltage and the AC small signal input voltage that we wish to amplify, the customary notation indicates DC voltages and currents with a *capital* V or I with a *capital* subscript, e.g., V_C or I_E. AC small signal quantities are indicated by a *small* v or i with a *small* subscript, such as v_{be} or i_b. Finally, a total voltage or current that is the sum of both DC and AC components is indicated by a *small* v or i with a *capital* subscript, like v_{BE} or i_C. So for the circuit of Figure 6.4, with the total input voltage (v_{BE}) given by the sum of the DC bias voltage (V_{BE}) and the small input signal (v_{be}), the collector current is given by

$$i_C = I_s e^{(V_{BE}+v_{be})/V_T},$$

which can be rewritten as

$$\begin{aligned} i_C &= I_s e^{V_{BE}/V_T} \cdot e^{v_{be}/V_T} \\ &= I_C \cdot e^{v_{be}/V_T} \end{aligned} .$$

This last equation expresses the total collector current (i_C) as a DC current (I_C) due to the DC input bias voltage multiplied by the small signal exponential. If we require that $|v_{be}| << V_T$, *then the exponent in the expression is a number less than one*. Now here is the neat trick: if we represent the exponential as an infinite series

$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \ldots$, where $x < 1$, we see that each of the terms in the series is much less than the sum of the preceding terms. For example, if the exponent is 0.2, the series is $1 + 0.2 + 0.02 + 0.00133 + 0.00006666 + \ldots = e^{0.2} \cong 1.2214$, which is approximately equal to 1.2, the sum of only the first two terms. So if we make the restriction that $|v_{be}/V_T| << 1$, then

$$e^{v_{be}/V_T} \approx 1 + \frac{v_{be}}{V_T} \qquad (v_{be} << V_T),$$

and we can express i_C as

$$i_C = I_C\left(1+\frac{v_{be}}{V_T}\right)$$
$$= I_C + v_{be}\left(\frac{I_C}{V_T}\right).$$

This last expression, known as the *BJT small signal model*, is what we need in order to use the BJT as an amplifier. It states that the total collector current (i_C) is the sum of a DC collector current component (I_C) due to the DC input bias voltage, and a *small signal collector current* component given by the product of the small signal input voltage (v_{be}) and the quantity I_C/V_T. **Note that as long as I_C and V_T remain constant and $|v_{be}| << V_T$, the small signal collector current is directly proportional to the input signal, v_{be}.**

This result can be expressed as $i_C = I_C + i_c$, where

$$i_c = g_m v_{be}, \text{ and}$$
$$g_m = \frac{I_C}{V_T} \text{ + } \textit{transconductance}.$$

The units of the transconductance, g_m, are amps/volt (reciprocal Ohms). The official unit of conductance is the *Siemen* (S), although you may sometimes see the casual term *mho* (pronounced 'mow') used.

Returning to the circuit of Figure 6.4, we can use the small signal model to determine the collector voltage (v_{OUT}) in terms of the input signal and the transconductance:

$$v_{OUT} = v_C = V_{CC} - R_c i_C$$
$$= \underbrace{V_{CC} - R_c I_C}_{V_{BIAS(DC)}} \underbrace{- R_c g_m v_{be}}_{v_{signal(AC)}}.$$

Finally, if we express v_{OUT} as the sum of the DC voltage (V_{CC} - R_cI_C) and the AC small signal voltage ($-R_cg_mv_{be}$), the *AC small signal voltage gain* (with no other load attached) for the circuit of Figure 6.4 is given by

$$\frac{v_c}{v_{be}} = -R_c g_m.$$

The negative sign indicates that this amplifier is *inverting*: the output voltage is an amplified and inverted version of the input signal. For example, if R_c happens to be 1kΩ, the thermal voltage (V_T) is assumed to be 25mV, and we adjust the DC bias so that I_C is 5mA, we can calculate

$$g_m = \frac{I_C}{V_T} = \frac{5\text{mA}}{25\text{mV}} = 0.2\frac{\text{A}}{\text{V}} = 200\frac{\text{mA}}{\text{V}}$$

and

$$\frac{v_c}{v_{be}} = -R_c g_m = -1\text{k}\Omega \cdot 200\frac{\text{mA}}{\text{V}} = -200$$

.

This means that for this example the AC output voltage will be 200 times larger than the AC small signal input voltage.

Separation of the DC Bias and AC Small-Signal Models

Strictly speaking, because the BJT is a nonlinear device we cannot apply the concept of superposition to analyzing amplifier circuits. However, the small-signal approximation developed in the last section allows us to treat the biased BJT as an AC small-signal linear device. The importance of this linearization is that we can use superposition to separate the DC bias and AC small-signal analyses of a BJT amplifier. Note that because the small-signal behavior of the circuit depends upon the DC bias conditions (e.g., g_m depends upon the DC bias collector current I_C), *we must always do the DC analysis first, then determine the correct parameters for the subsequent AC small-signal analysis*.

Once the DC bias conditions are determined, the appropriate small-signal model for the circuit can be applied. One common small-signal model is the *hybrid-π* model, named because it looks a little bit like the Greek letter π. The simplified hybrid-π model for the biased BJT is shown in Figure 6.5.

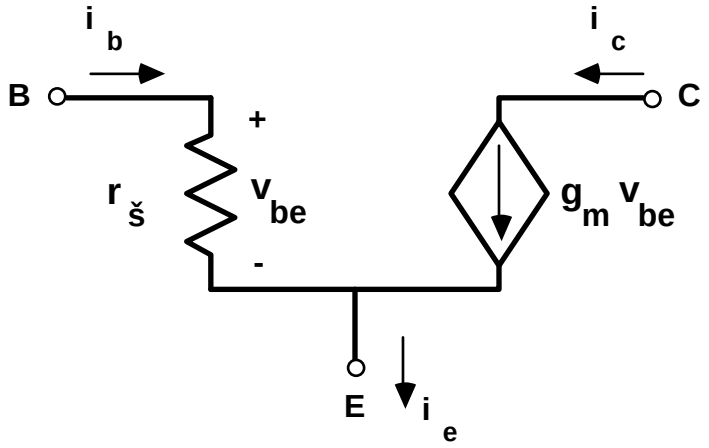


Figure 6.5

The resistor r_π is the *equivalent small-signal base input resistance*. Using the small-signal model equations we see that

$$v_{be} = r_\pi i_b$$
$$i_c = \beta i_b = g_m v_{be}$$

and

$$r_\pi = \frac{\beta}{g_m} = \frac{\beta V_T}{I_C} = \frac{V_T}{I_B} .$$

The simplified hybrid-π model of Figure 6.5 can be made more accurate by adding an *equivalent small-signal collector output resistance*, r_o, in parallel with the model's controlled current source. The small-signal output resistance is given by

$$r_o = \frac{V_A}{I_C} ,$$

where V_A is the Early voltage, described previously. Notice that like g_m, both r_π and r_o depend upon the DC bias conditions (I_C) of the transistor.

Since we want to separate the amplifier analysis into DC and AC portions, we must remember that all DC circuit components, such as DC power supplies, appear *only* in the DC analysis. When the AC analysis is performed all DC quantities appear as their Thévenin equivalent AC impedances. For example, the DC supply V_{CC} in Figure 6.4 is used when determining the DC bias currents and voltages, *but it becomes a short circuit to*

ground in the AC analysis since the Thévenin AC impedance of a DC voltage source is zero.

Hand Analysis of BJT Amplifier Circuits

When performing a hand analysis of a BJT amplifier circuit, the initial DC analysis is typically handled using the following procedure:

DC ANALYSIS
• Assume the BJT is in the active mode (and check this assumption later!) • Assume the base-emitter voltage is 0.7 volts and obtain the approximate β parameter (or choose a reasonable β value, say, 50-100). • Calculate the DC terminal currents and voltages using Ohm's law and the basic BJT equations. • Finally, verify that the circuit is indeed in the active mode (correct junction voltages).

Although this is a rather simple approach which involves several imprecise assumptions, it usually suffices for quick "go / no-go" examinations. More careful analysis can always be done using a SPICE simulation or measurements on a prototype circuit.

Once the DC bias conditions are determined we can calculate the small-signal parameters (g_m, r_π, and r_o) for use in finding the AC small-signal voltage gain, etc.

AC ANALYSIS
• Use the DC bias conditions to calculate the AC small-signal parameters: $g_m = \frac{I_C}{V_T}, \quad r_\pi = \frac{\beta V_T}{I_C}, \quad r_o = \frac{V_A}{I_C}$. • Use the AC small-signal equivalent circuit (e.g., hybrid-π) to find the input and output characteristics of the amplifier.

BJT Amplifier Design Considerations

A basic common-emitter BJT amplifier configuration is shown in Figure 6.6.

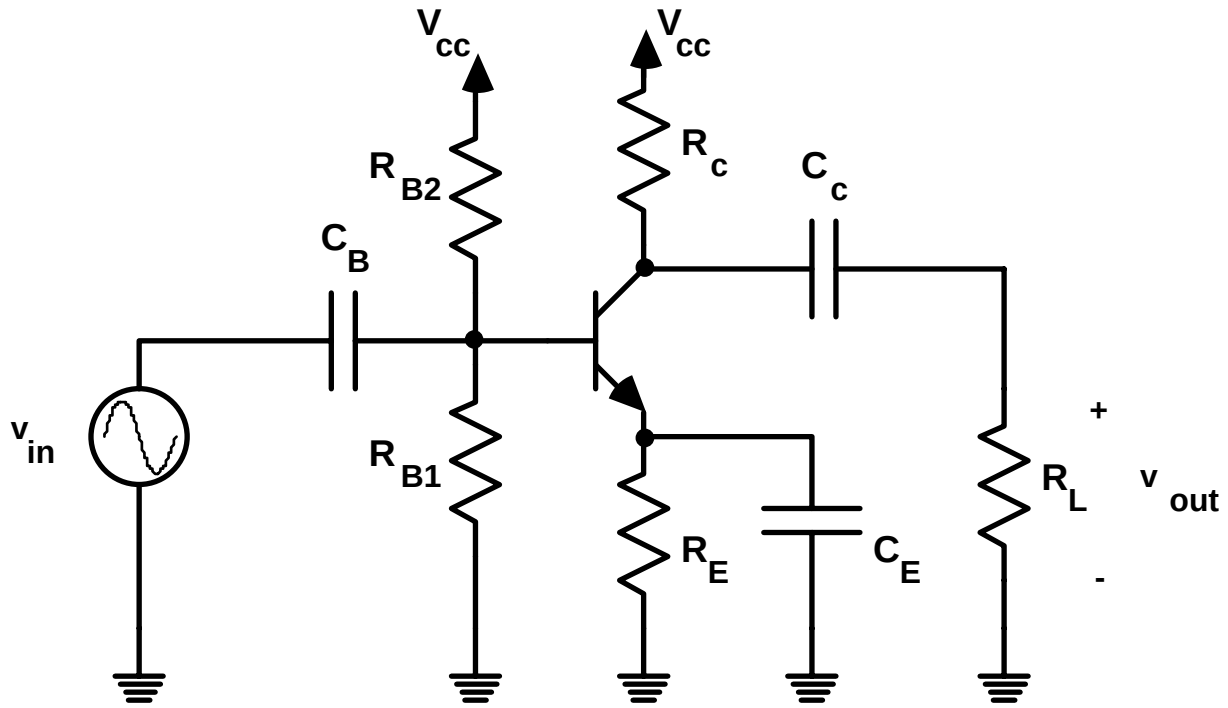


Figure 6.6

The circuit is comprised of a BJT with four resistors (R_{B1}, R_{B2}, R_C, and R_E) used to establish the correct DC bias conditions, and three capacitors (C_B, C_C, and C_E) to block any DC disturbance of the bias conditions while still allowing the AC signals to pass through the amplifier. The capacitor values are chosen so that their impedance magnitude ($1/\omega C$) is small over the AC frequency range to be amplified, and essentially infinite at DC ($1/0 \varnothing \square$). *For our purposes we will assume that the capacitors can be treated as open circuits for the DC analysis and are large enough that they can be treated as short circuits for the AC analysis.* This assumption allows us to consider the DC analysis using the circuit of Figure 6.7, and the AC analysis using the circuit of Figure 6.8.

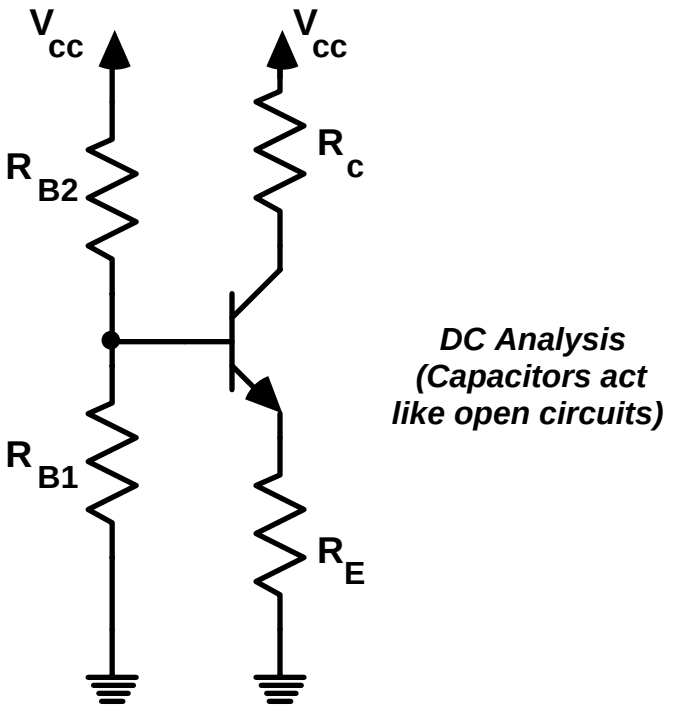


Figure 6.7

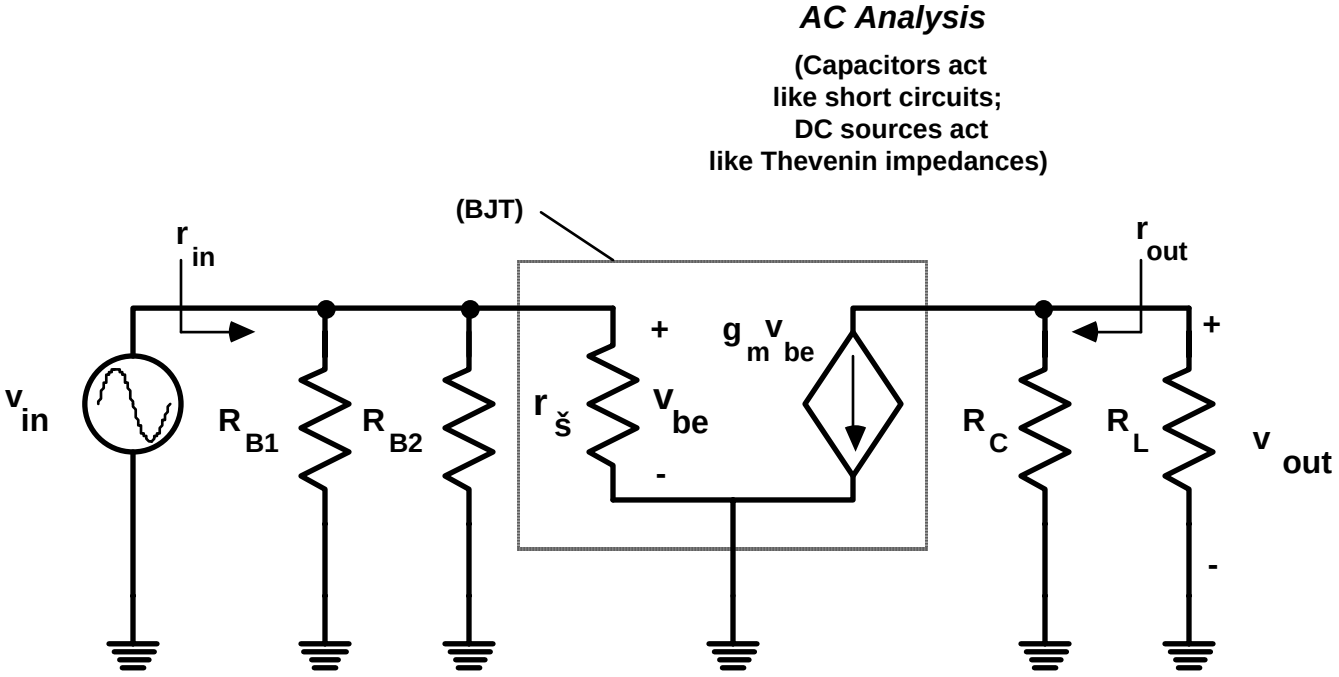


Figure 6.8

Notice that the DC supply (V_{CC}) is used in the DC analysis only, and becomes its AC Thévenin equivalent–*an AC short circuit*–in the AC analysis. In other words, the DC supply does not appear in the AC model because it has already been taken into account during the DC analysis.

Also note that R_E does not appear in the AC model because it is "shorted out" by the parallel capacitor, C_E. R_E is included in the circuit because it acts as a stabilizing element: if the DC emitter current should change due to a temperature shift, a different value of β, or some other effect, the voltage across R_E changes, too, since $V_E = I_E R_E$. This change in V_E tends to cause a complementary change in V_{BE}, i.e., a decreasing emitter current tends to lower V_E and *increase* V_{BE}, thereby causing the emitter current to increase due to the exponential relationship between the emitter current and the base-emitter voltage. Thus, R_E acts as a *negative feedback* for any changes in the circuit's bias conditions. This helps make the circuit less sensitive to the exact value of the transistor parameters, resulting in a design that is easier to manufacture. Nevertheless, you should notice that the inclusion of R_E is not without a drawback: it reduces the maximum output voltage swing of the collector since v_{CE} must be > 0 to remain in the active region.

From Figure 6.8 we can obtain several of the AC small-signal characteristics of this amplifier.

- The effective *AC input resistance* (r_{in}) seen by v_{in} is the parallel combination of R_{B1}, R_{B2}, and r_π, since all three of those components are connected from v_{in} to ground in parallel.

- The effective *AC output resistance* (r_{out}) seen by the load resistor, R_L, is simply R_C since the output resistance of the controlled current source is infinite.

- The *AC voltage gain* (v_{out}/v_{in}) with R_L attached is $-g_m(R_C||R_L)$, since for this circuit $v_{be} = v_{in}$ and the current $g_m v_{be}$ is pulled through $R_C||R_L$ in the negative direction with respect to the definition of v_{out}.

In choosing the value of the four bias resistors we must make several design decisions. For example, we would like to make the DC bias conditions for the circuit relatively independent of the exact value of β for the transistor, since β tends to vary from device to device and depends upon temperature and other effects. This can be achieved if the voltage at the base of the BJT can be made as independent of the base current (I_B) as

possible. One way that this can be accomplished is to choose R_{B1} and R_{B2} so that the currents through those resistors are much greater than the base current. Unfortunately, large DC currents in R_{B1} and R_{B2} increases the total power dissipated by the circuit, which is usually undesirable, particularly if V_{CC} is a low-power battery.

The appropriate resistor values can be determined once the desired DC collector current or emitter current ($I_C \approx I_E$) is chosen. The choice of collector current is typically made as a tradeoff between the desirable higher voltage gain available with large I_C, and the similarly desirable decrease in DC power dissipation and increase in input impedance available with small I_C. The appropriate tradeoff will depend upon the requirements of the design. One common approach for selecting the DC bias conditions is to set the base voltage at $V_{CC}/3$ and the collector voltage at $2V_{CC}/3$, leaving $V_{CC}/3$ - 0.7 volts for the emitter voltage. This choice provides the greatest possible signal swing at the collector: the total output signal at the collector can swing to a maximum of V_{CC} and a minimum of $V_{CC}/3$ ($2V_{CC}/3 \pm V_{CC}/3$), while still remaining in the active mode as required for a linear BJT amplifier.

A summary of the basic guidelines for choosing the DC biasing resistors are:

• Choose the required collector (or emitter) current for the desired DC bias conditions and small-signal gain.
• Choose R_C so that $V_C \approx \frac{2}{3} V_{CC}$ (which implies $I_C R_C \approx \frac{V_{CC}}{3}$).
• Choose R_{B1} and R_{B2} so that $V_B \approx \frac{V_{CC}}{3}$, and $\frac{V_{CC}}{(R_{B1} + R_{B2})} \approx \frac{I_E}{2}$.
• Choose R_E so that V_{BE} = 0.7 volts (which implies $I_E R_E \approx \frac{V_{CC}}{3} - 0.7$).

BJTs and SPICE

SPICE includes an extensive BJT model. The model implements the basic bipolar junction transistor equations, with the symbol **IS** for I_s, **BF** for β, and **VAF** for the Early voltage, V_A. A BJT is declared in SPICE as:

```
Qname   NC NB NE  modelname
...
.MODEL  modelname  type  (IS=xx, BF=yy, VAF=zz)
```

where *NC*, *NB*, and *NE* are the node numbers connected to the collector, base and emitter, respectively. The name of the BJT (**Q***name*) is up to you, except that the first letter must be a **Q**, and you are also free to choose *modelname*, the name of the model. The *type* is either **NPN** or **PNP**.

The SPICE BJT model has numerous other parameters that are used to describe the operation of BJTs in various configurations, frequency ranges, etc. The library of device models supplied with the student version of PSpice (EVAL.LIB) contains several more complete transistor models for actual transistors.

Discrete BJT Packaging

Discrete BJTs come in various shapes and sizes. The smallest discrete BJTs for low-power applications are roughly the size of an aspirin tablet, and are mounted in a metal canister or encased in a plastic or epoxy button. Devices designed for high-power operation (greater than a watt or two) are generally mounted in a larger metal package that includes screw holes for attaching the entire package to a metal heat sink. This improves the rate at which heat is dissipated from the device, thereby preventing the transistor from burning up. The emitter is sometimes identified by a tab or index mark, but often it is necessary to refer to a manufacturers data book or simply to test the terminals to identify the forward direction of the *pn* junctions: the junctions will conduct negligible current when in reverse bias and an approximately fixed voltage drop in the forward bias direction. Several example packages are shown in Figure 6.9. Many types of transistors (including BJTs) are often given a standard part number beginning with '2N', e.g., 2N2222, 2N3904, etc.

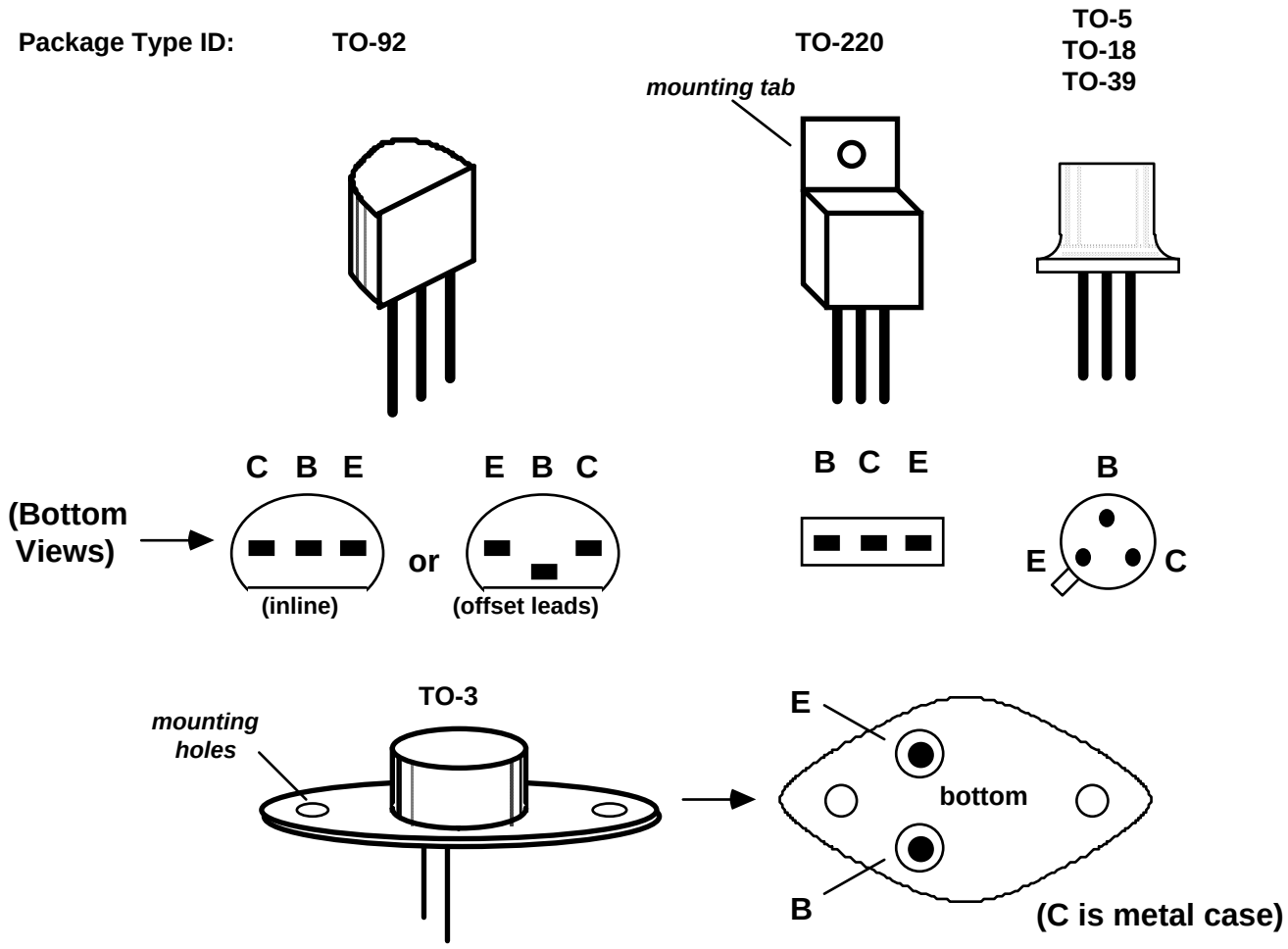


Figure 6.9

It is also possible to purchase compound circuits consisting of several BJTs mounted in a single package. These circuits are used where precisely matched transistors are required, or to simplify the layout and assembly of BJT circuits by reducing the number of individual components that must be handled.

A Few Words About Electrolytic Capacitors

The DC blocking capacitors used in the BJT amplifier design must often be large in value (tens or hundreds of microfarads). Since large values of capacitance require large plate area, these capacitors tend to be physically large and expensive if they are manufactured from conventional ceramic or film materials. An alternative method to obtain large capacitance values is to use *electrolytic* capacitors. As the name implies,

electrolytic capacitors are constructed of electrodes immersed in a paste of electrolyte, a chemically conducting material. An oxide on one of the electrodes provides dielectric (insulating) separation. These devices provide high capacitance values in relatively small containers. The 22μF capacitors used in this experiment are electrolytic.

There are some important things to keep in mind when using electrolytic capacitors. Electrolytic capacitors are usually *polarized*, meaning that you *must* ensure that the voltage is applied to the capacitor in a particular polarity. Connecting an electrolytic capacitor backwards can be damaging since large currents can flow through the device. Thus, be sure to observe the correct polarity when assembling your circuits! Another important consideration is that electrolytic capacitors generally have relatively poor tolerance (typically ±20% or worse). This is usually not a problem in DC blocking applications, since we want the capacitor to be "big enough" to pass the AC signals but we don't really care exactly how big.

REFERENCES

See Chapter 4 of the text by Sedra and Smith, *Microelectronic Circuits*, 3rd ed., Saunders College Publishing (Holt, Rinehart, and Winston), 1991.

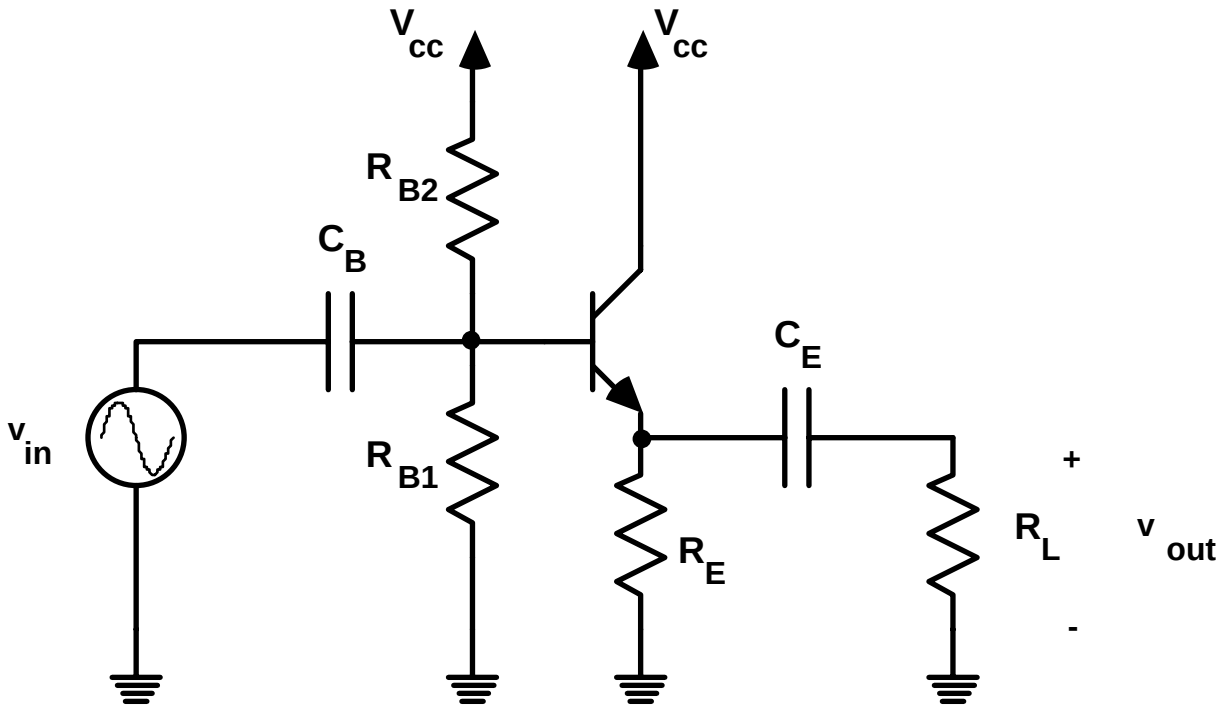
EQUIPMENT

Lab component kit (resistors, capacitors, BJTs)

Digital Multimeter (DMM)	Power supply	Function generator
Oscilloscope	Heathkit trainer	

PRE-LAB PREPARATION

(I) Consider the circuit of Figure 6.10 below. The circuit is called an *emitter-follower*. *Remember*, you need to determine the DC bias conditions first, then calculate the AC small-signal parameters. Assume that the capacitors are DC open circuits and AC short circuits, and also assume that V_{BE} is 0.7 volts and $\beta \geq 80$ for the DC portion of the analysis.



R_{B1} = 10kΩ R_{B2} = 33kΩ
R_E = 1kΩ R_L = 300Ω
V_{cc} = +15volts (C_E, C_B ∅ □)

Figure 6.10

From the DC bias conditions and the small-signal model, calculate the AC input and output resistance (seen by v_{in} and R_L, respectively), the small-signal voltage gain, and the AC power gain { power gain = (AC power delivered to load resistor, R_L)/(AC power supplied by input source, v_{in}) }.

Compare the gain and impedance characteristics of the emitter-follower to the common-emitter amp considered previously (the emitter-follower is often used to *buffer* a high-impedance source driving a low-impedance load).

(II) Choose component values for the common-emitter circuit of Figure 6.6 according to the following specifications:

- Assume V_{BE} = 0.7 volts and β = 80 (DC).
- V_{CC} = 18 volts.
- V_C (DC) ≈ 12 volts, V_B (DC) ≈ 6 volts.

- Small-signal voltage gain magnitude must be ≥ 60 (in the passband).
- R_L = 2.2kΩ.
- AC small-signal input resistance (seen by v_{in}) must be ≥ 360Ω (attempt to maximize).
- AC small-signal output resistance (seen by R_L) must be ≤ 2.2kΩ (attempt to minimize).
- Assume capacitors C_B, C_C, and C_E are open circuits at DC and short circuits for AC.

If standard nominal resistor values (from the 5% tolerance list) are to be used, can all the specifications be met? Explain your design choices.

(III) Use SPICE and PROBE to perform a DC analysis (`.DC`) and AC sweep analysis (`.AC`) of the common-emitter amp using the component values you calculated in part (II), for β=20, 80, and 200. Perform the AC sweep over the frequency range 20 Hz to 200kHz. Use 22μF capacitors for C_B, C_C, and C_E. Except for the specified values of β, use the default SPICE BJT model parameters. Note that you should expect the AC sweep to show a gain characteristic that starts small for low frequencies and increases asymptotically to a maximum level.

- What effect does the change in β have on the DC bias operation?

- What is the maximum gain for each of the three values of β?

- Below what frequency does the gain in each case become more than 3 dB less than the maximum value? Recall that *dB* for voltage gain is given by $20 \log_{10}|\text{gain}|$.

(IV) Consider the op amp and BJT circuit shown in Figure 6.11. This circuit is referred to as a *current booster* configuration because the output current capability of the op amp (typically < 30mA) is boosted by the current gain of the BJT. This configuration buffers the positive input signal, allowing a low-power source to control a large, positive current in the load resistor.

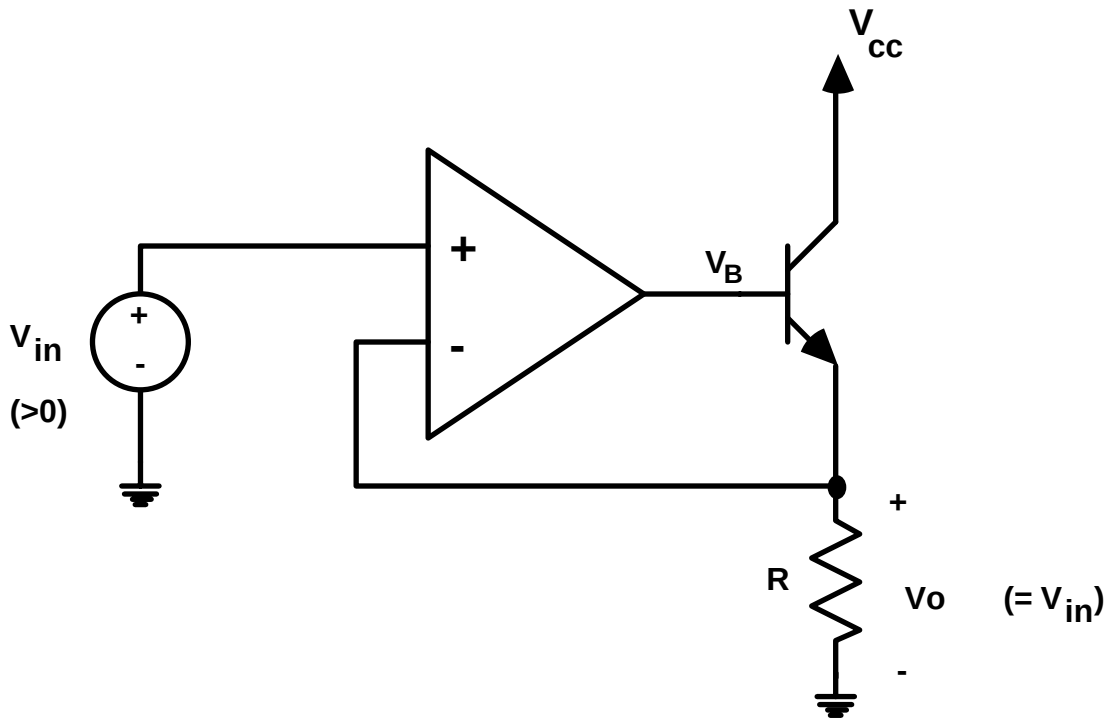


Figure 6.11

Observe that the current in the load resistor, R, is ideally equal to the emitter current of the transistor. As long as the BJT is in the active mode the emitter current is $(\beta+1)\cdot I_B$, with the additional current coming from the collector supply, V_{cc}, instead of from the op amp output. Note that the inclusion of the BJT in the negative feedback path of the op amp forces V_o to be equal to V_{in}: the output voltage of the op amp adjusts V_{BE} until the voltage difference between the inverting and noninverting inputs goes to zero (ideally).

(i) Sketch V_o vs. V_{in} and V_B vs. V_{in} on the same graph for $V_{in} > 0$. Assume $V_{BE} \approx 0.7$ volts when the transistor is "on".

(ii) If the maximum output voltage of the op amp is +12 volts and the maximum op amp output current is 12mA, what is the smallest resistor, R, that can be used in this configuration if β=20? If β=80? If β=120? How does this compare to the smallest resistor value if the op amp output was attached directly to R, without the BJT booster? Again, assume $V_{BE} \approx 0.7$ volts.

EXPERIMENT

(1) Use the multimeter to verify the terminals of the BJTs in your lab kit. Use the "diode" test setting of the meter to determine the forward junction directions. Note that if a pair of BJT terminals shows a high impedance for either direction of the test leads, that pair must be the collector and emitter. For an NPN transistor (such as the 2N2222) the base∅collector and base∅emitter junctions *may* be distinguishable because the forward voltage of the BC junction is sometimes less than for the BE junction for a constant current from the diode tester.

(2) Select a BJT from you kit and measure and plot I_C vs. V_{CE} for I_B =10, 20, and 50 μA over the range $0 \le V_{CE} \le 10$ volts, using the test configuration of Figure 6.12. Adjust power supply V_1 to set the desired value of I_B, and adjust V_2 to set the desired value of V_{CE}. Note that $I_B = V_{RB}/R_B$ and $I_C = V_{RC}/R_C$, so determine the currents by measuring the voltages.

How does the value of beta ($\beta = I_C/I_B$) vary for different values of I_B and V_{CE}? Also, estimate the value of V_A for the transistor.

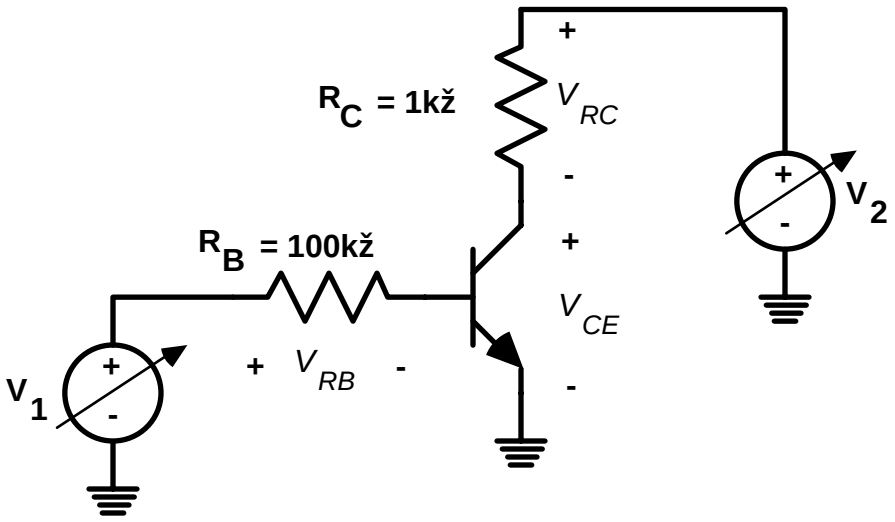


Figure 6.12

(3) Now measure the I_C vs. V_{CE} for the BJT using the curve tracer instrument in the lab. Compare the results to your hand measurements from part 2.

(4) Construct the common-emitter amplifier you designed in section II of the pre-lab. OBSERVE THE CORRECT POLARITY FOR THE ELECTROLYTIC CAPACITORS!

Carefully measure the DC bias conditions and compare to your SPICE analysis and the design specifications. Measure and record the voltage gain of the circuit for sinusoidal input with frequencies in the range 100 Hz through 200kHz. *Remember* to keep the input signal small enough so that the output does not become distorted. Try different input amplitudes and observe the quality of the output waveform. Try some different resistors for R_C and R_L and observe how the characteristics of the circuit change.

(5) Construct the current-booster circuit of Figure 6.11 using an op amp from your lab kit. Power the op amp using the Heathkit trainer and use the bench supply to provide V_{CC} = 15 volts for the transistor. Use R=100Ω and vary V_{in} from 0 to 5 volts in several steps. Measure I_B, V_B, and V_o at each step.

(6) Finally, feel free to construct the emitter-follower circuit from the pre-lab, or experiment with the various circuits considered in this experiment.

RESULTS

(a) Identify the package type and the identity (base, collector, and emitter) of the BJT terminals from part 1. Were you able to identify the device? How would your verification differ if the BJT was PNP instead of NPN?

(b) Present your I_C measurements and graphs from parts 2 and 3. How do your hand measurements and curve tracer results compare? What range of β values did you calculate? What value of V_A do you estimate for the BJT?

(c) Describe your measurements of the common-emitter amplifier you constructed in part 4. Present your voltage gain vs. frequency measurements. Describe your observations with different input amplitudes and resistor values. Compare your lab results with your pre-lab predictions and SPICE simulations.

(d) Present your measurements for the current-booster circuit. Give your measurements of V_{in}, I_B, V_o, along with calculations of the transistor β, the load current, and the load power. Compare your results to your expectations based on the pre-lab work.

(e) Did you attempt to construct any other circuits or make any other circuit modifications? Describe what you learned.

(f) What parts of this experiment should be changed to make them more clear?

Revised 7/94

Lab # 7
TITLE: Electrical Resonance and Resonant Circuits

ABSTRACT

The concept of electrical resonance is important in the analysis and design of many types of electronic circuits. This experiment considers the resonant behavior of **parallel** RLC circuits. Although only series circuits are considered here, the **series** RLC circuit is the **dual** of the parallel and may be analyzed in much the same way. Measurements of magnitude and phase response of resonant circuits are performed and the results compared to the computer (PSpice) simulations. The Q (quality factor), ω_o (center frequency), BW (bandwidth), and half-power frequencies (ω_{LO} and ω_{HI}) are demonstrated through the design and construction of a simple RLC parallel resonant circuit.

INTRODUCTION AND THEORY

In an earlier experiment (#1) the response of a series RLC circuit was examined. That earlier experiment showed the total solution was a combination of the natural and forced solutions. At that time only DC forcing functions were discussed. A much more interesting problem is the solution for a sinusoidal forcing function. The sinusoidal input is assumed to have been applied for a long time such that the natural response is negligible. This solution is very important because, by using **Fourier analysis**, the solution for any periodic forcing can be found as the sum of solutions of sinusoidal functions of certain frequencies and amplitudes. Fourier analysis is discussed in chapter 18 of the Irwin text but will be covered more extensively in several future EE courses (especially EEngr 304, & EEngr 462).

The sinusoidal solutions for series and parallel RLC are quite similar. The resistor current magnitude is maximum (minimum) at resonance for the series (parallel) RLC circuit. At resonance the phase angle between the resistor voltage and source voltage for the **series** circuit and phase angle between the resistor current and source current for the **parallel** circuit is always zero. Depending on whether the operating frequency is **above or below** the resonant frequency, the phase angle is negative or positive (always with respect to the source variable). In this lab you will measure the phase angle of the resistor voltage with respect to the source current, and the current magnitude for a parallel RLC circuit across a range of frequencies including both half power points and the resonant frequency. The Q (quality factor) of the circuit will also be calculated. Also note the inverse relationship between the Q (quality factor) and the bandwidth (BW). The Q of a circuit is also important in acoustical and mechanical systems where

the more general definition becomes $Q = 2\pi \frac{W_S}{W_D}$, where W_S is the maximum energy stored at resonance and W_D is the energy dissipated per cycle.

REFERENCES

See section 14.3 of the text by J. David Irwin, *Basic Engineering Circuit Analysis*, 4th ed., Macmillan Publishing Co., 1993.

EQUIPMENT

Lab component kit
0.5 H inductor (variable 0.1 to 1.0 H) Sine wave generator
Multimeter (RMS) Oscilloscope
Heathkit Trainer (or breadboard)

PRE-LAB PREPARATION

(I) Calculate the transfer function [V_o/I_{in}] for the circuit of Figure 7.1. Solve for magnitude and phase in terms of ω, ω_o, and Q. Since we will be referencing our measurements to I_{in}, does R_{cl} have any effect on the circuit?

Next, calculate values for ω_{HI}, ω_{LO}, ω_o, and Q. Make a table which shows how increasing/decreasing the value of each circuit component affects the parameters.

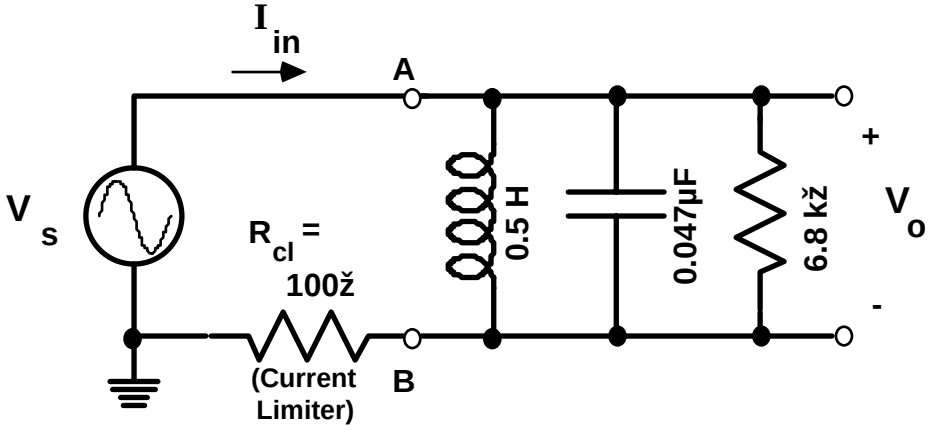


Figure 7.1

(II) Perform an AC PSpice analysis (600-1300 Hz) of the RLC portion of Figure 7.1 using a current source for the excitation. Recall that PSpice current sources are defined with positive current flowing *into* the positive terminal and *out of* the negative terminal.

(a) Generate a Probe graph of current magnitude (I_R) vs. frequency. Label the resonant frequency and half-power frequencies.

(b) Generate Probe graphs of both phase and relative magnitude vs. frequency for the transfer function [V_o/I_{in}].

(c) Consider the effect of the non-zero internal resistance of a real inductor on the response of the circuit. How will this change the behavior of the circuit?

(III) Design a circuit similar to Figure 7.1 which has a band-pass transfer function [V_o/I_{in}] with a center frequency (f_o) of 2 kHz and a bandwidth ≤ 500 Hz. You will assemble this circuit in the lab so components must be in your lab kit or otherwise available to you. NOTE: A variable inductor (0.1 to 1.0 by 0.1 H increments) will be available in the lab.

(a) Draw your design and list nominal values of components selected. Parts catalogs (such as Digi-Key) show standard values available for resistors and capacitors.

(b) Analyze your design using PSpice as in part (II).

EXPERIMENT

(1) Use the inductance/capacitance meter to accurately measure the values of the components you selected for your design (in part III of the pre-lab). Use the multimeter to measure the resistor and the internal resistance of the inductor.

(2) Connect the circuit of Figure 7.1 but use the components you selected in the pre-lab. Connect the sine generator and adjust the level so that I_{in} = 50μA (rms).

(a) Referring to the previous experiments in which phase angle was measured, use the method of your choice to determine the phase angle between V_o and I_{in}. Also, use the multimeter to measure the rms voltage across the inductor, resistor, and capacitor. Perform the measurements every 50 Hz. Be sure to cover the **entire bandwidth** (plus a little extra) of your circuit. Measure the sine generator output every time the frequency is varied *and re-adjust so that I_{in}= 50μA (rms) if necessary*. Also be careful measuring the sign of the phase. Does V_o lead or lag I_{in}?

(b) Use the value of the maximum gain of $|V_o/I_{in}|$ to calculate the half power points ω_{LO} and ω_{HI}. Ensure your data includes both half power points before disassembling the circuit.

(c) All lab results should be repeatable, and the techniques used comprehensible, from reading the lab notebook. The equipment setup (especially the oscilloscope hookup) should be sketched and explained.

RESULTS

(a) Plot the results of part (2) of the lab. Plot gain magnitude vs. frequency and phase angle vs. frequency for your RLC design circuit. Label the resonant frequency, half power frequencies, and the bandwidth.

(b) Compare the pre-lab results (using PSpice) with the lab results. Did you meet the design requirements and if not, why? Discuss the effect of the internal resistance of the inductor and the effect of differences in nominal and actual component values.

(c) What is the relationship between Q and the bandwidth (BW)?

(d) Use your measurements at the half-power frequencies to graphically determine the phase angle of (V_o/I_{in}) using a phasor diagram.

(e) Discuss which technique you used to measure the phase angle and why you used that method.

(f) What can be done to improve this experiment?

Revised 7/94

Lab # 8
TITLE: Metal-Oxide-Semiconductor Field-Effect Transistors

ABSTRACT

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are used in many applications where the high MOSFET gate impedance is an asset. This experiment deals with several important features of MOS transistors and transistor circuits. In addition, the use of MOSFETs in switching circuits is considered.

INTRODUCTION AND THEORY

The MOSFET ("mmahhs-fehht") is a three-terminal device in which the voltage between two of the terminals controls the current flowing in the third terminal. Like the BJT, this means that MOSFETs can be used as controlled current sources in the design of signal amplifiers and digital circuits. The material in this introduction is only intended to be a summary of MOSFET concepts. Refer to your EEngr 260 textbook for a more careful treatment.

MOSFETs consist of two back-to-back *pn* junctions separated by a *channel* region. Above the channel region an insulating oxide is used to separate a conductive electrode from the semiconductor channel material, as shown in Figure 8.1.

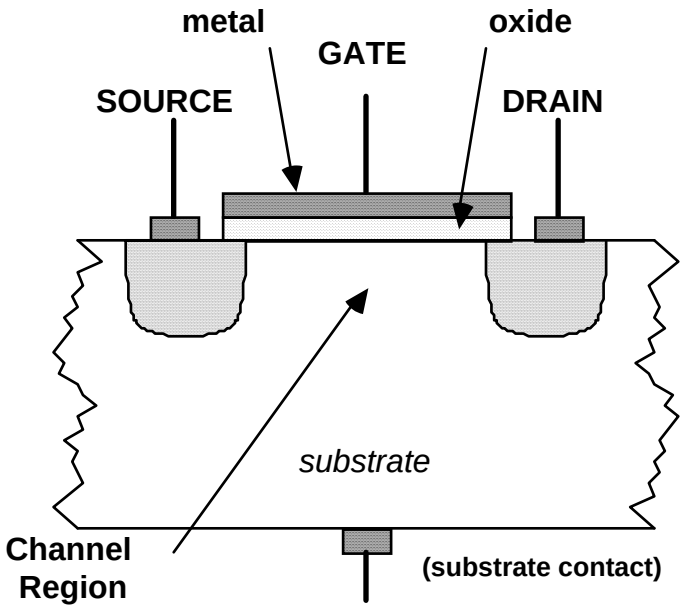


Figure 8.1

The metal - oxide - semiconductor sandwich across the channel is the origin of the *MOS* in the MOSFET acronym. As indicated in the figure, MOSFETs can be fabricated either with a *p*-type or *n*-type substrate material.

The electrical connections at the ends of the channel are known as the *drain* and the *source*, while the electrode overlying the channel is called the *gate*. In normal operation current flows between drain and source through the channel material. The physical distance from between the drain and the source is referred to as the *channel length*, L. The other rectangular dimension of the region under the oxide is referred to as the *channel width*, W. The ratio of the channel width to the channel length (W/L) is an important parameter under the control of the MOSFET designer because it varies the conducting properties of the device.

Simplified MOSFET Description

An immediate question must be the following: how can conduction occur between drain and source, since there are oppositely polarized *pn* junctions between drain and channel and between channel and source? The answer is that *there cannot be drain to source conduction unless a conducting channel is formed*. The conductive channel can either be built-in by fabricating a layer of material with the same semiconductor properties as the drain and source material (*p* or *n*), or by *inducing* a channel using the gate electrode. Devices with a built-in channel are referred to as *depletion MOSFETs* because the built-in conduction between drain and source can be reduced (or *depleted*) using the gate electrode, while devices without a built-in channel are referred to as *enhancement MOSFETs* since the gate electrode can be used to increase (*enhance*) the conductive properties of the device.

How does the gate affect conduction? Note that although the gate is electrically insulated from the channel by the gate oxide so that no DC current flows in the gate electrode, it *is* possible for the gate to influence the channel material if a voltage difference--and thus an *electric field*--exists across the oxide. The presence of an electric field due to the gate allows control of conduction between drain and source, hence the *field-effect* descriptor in FET. Also, observe that the metal - oxide - semiconductor sandwich acts something like a parallel plate capacitor, where the oxide is the dielectric material.

In the case of an *enhancement* device with a *p*-type substrate, the gate must be driven to a *positive* voltage with respect to the channel material, thereby *repelling* the mobile *p*-type

carriers ("holes") from under the oxide and leaving behind the negative fixed charge of the substrate atoms. The positive gate voltage also acts to *attract* mobile *n*-type carriers (electrons) from the source and drain regions into the channel area under the oxide. *If sufficient positive bias is applied to the gate electrode, a conducting n-type channel is induced under the gate oxide and current can be conducted from drain to source*. Thus, this type of device is called an *n*-channel enhancement MOSFET: *enhancement* because the conduction is enhanced by the gate, and *n-channel* because an *n*-type channel is induced. This is often abbreviated *enhancement NMOS*.

A similar effect occurs in the case of *n*-type substrate material, except the gate is driven to a *negative* potential so that a *p*-type channel is induced under the oxide. This type of device is called a *p*-channel enhancement MOSFET, or *enhancement PMOS*.

Depletion devices, on the other hand, usually use the gate voltage to deplete the mobile carriers in the built-in channel. For example, an *n*-type channel is depleted by applying a negative voltage to the gate with respect to the substrate material, thereby repelling the mobile *n*-type carriers (electrons) in the channel region and reducing conduction.

Cross-section representations of the *n*-channel and *p*-channel MOSFET devices are depicted in Figure 8.2a and 8.2b, respectively, along with the common circuit symbols for the devices.

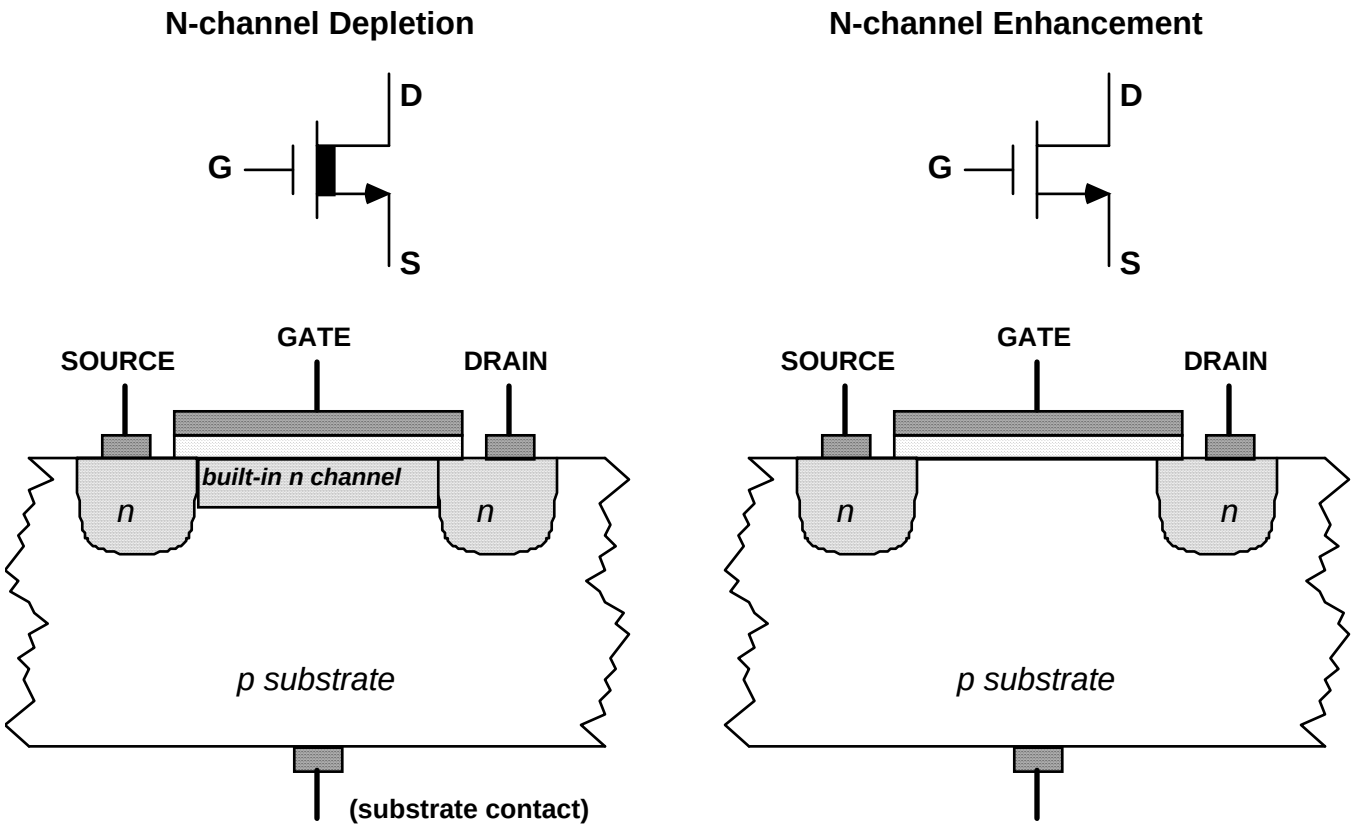

N-channel Depletion
N-channel Enhancement
D
G
S
D
G
S
SOURCE
GATE
DRAIN
built-in n channel
n
n
p substrate
(substrate contact)
SOURCE
GATE
DRAIN
n
n
p substrate

Figure 8.2a

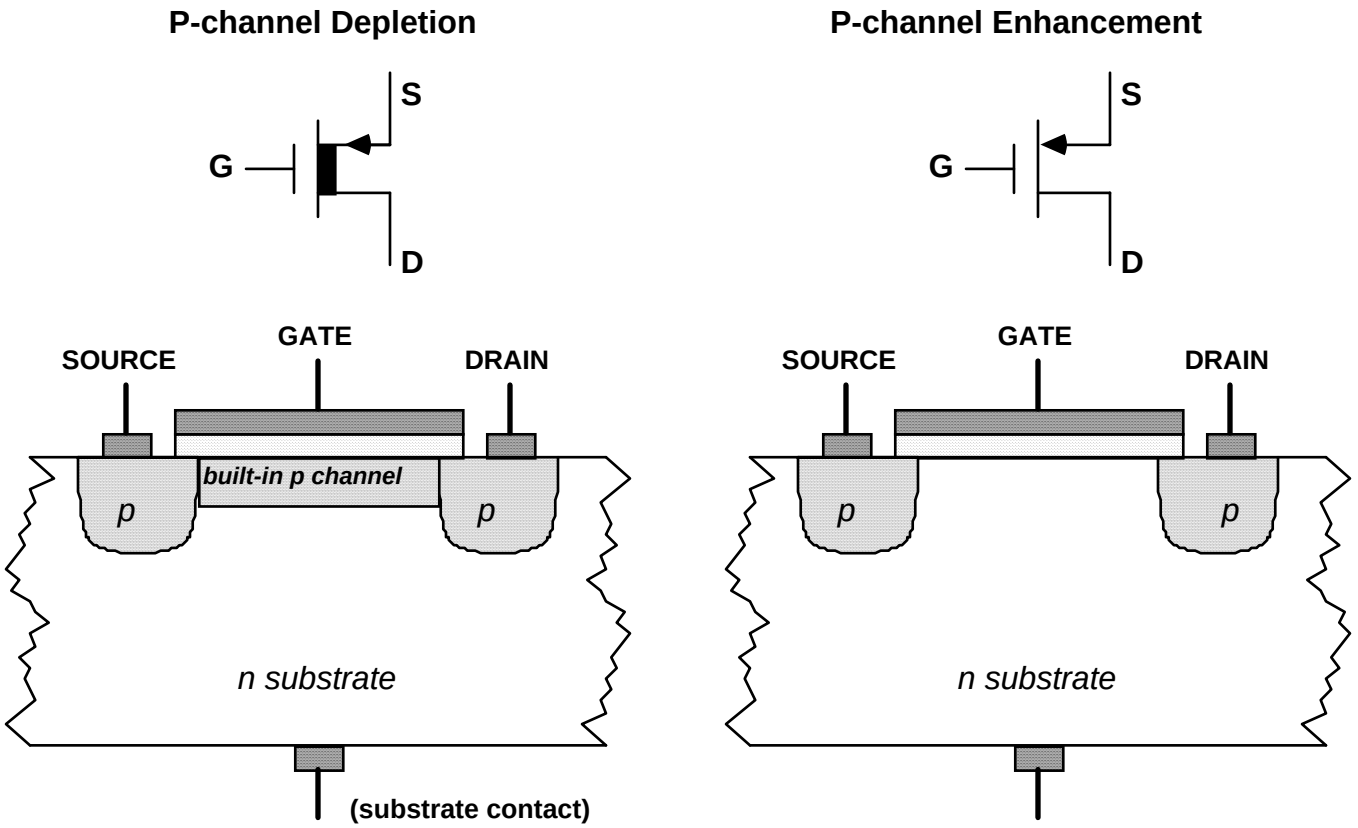


Figure 8.2b

The schematic symbols for the *depletion* MOS devices can be distinguished by the wide vertical band representing the built-in channel between the drain and source terminals. The *n*-channel and *p*-channel devices are distinguished by an arrow symbol pointing *out* for the *n*-channel symbol, and *in* for the *p*-channel symbol. Note that the arrow is always on the source lead, and its direction indicates the forward *pn* junction direction, i.e., from substrate to source for *n*-channel, and from source to substrate for *p*-channel. Also notice that the *n*-channel symbols are typically drawn with the drain on top since the normal current direction is from drain to source, while the *p*-channel symbols have the source on top, since the normal current direction for *p*-channel devices is from source to drain. This keeps the current flowing symbolically from the top of the page to the bottom.

In many discrete transistor applications the substrate is electrically connected to the source. There are many situations, however, where the substrate and source are not connected and the substrate contact must be shown explicitly. The typical symbols including the substrate terminal are shown in Figure 8.3. Notice that built-in channel of

the depletion devices is indicated by a solid vertical bar, while the enhancement devices have a broken vertical bar. The direction of the substrate arrow indicates the channel type, since the arrow points from *p* to *n* type material (e.g., from *p* substrate toward *n* channel for NMOS). Also note that the gate terminal is often drawn closer to the source terminal simply for notational convenience.

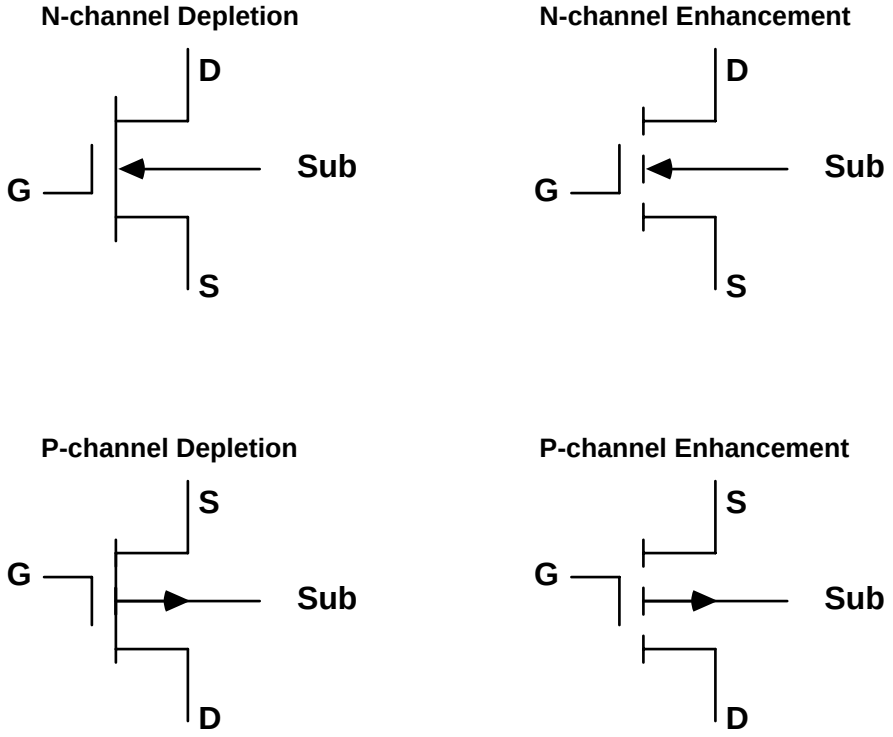


Figure 8.3

Unlike BJTs, where the collector and emitter junctions are fabricated differently, most actual MOS devices are essentially bi-directional with the drain and source being interchangeable. In fact, there are many switching applications in which the bi-directional properties of MOSFETs are very useful. As mentioned, however, discrete transistors often have the substrate terminal and the labeled source terminal internally connected.

Channel Behavior of the Enhancement MOSFET: Triode and Saturation

Consider the *n*-channel enhancement MOSFET circuit of Figure 8.4. Again, we will use subscripts to denote voltage differences, such as $v_{DS} = v_D - v_S$. Since the gate current i_G must be essentially zero due to the insulating gate oxide, notice that the current i_S

leaving the device must be equal to the current i_D entering at the drain (Kirchhoff's Current Law).

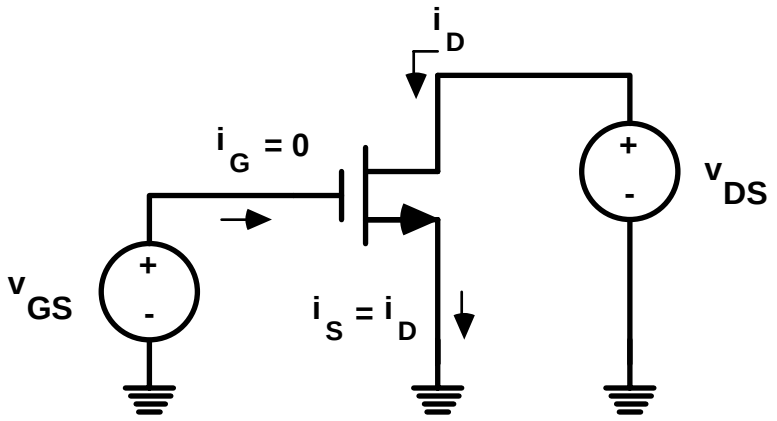


Figure 8.4

If we set v_{DS} to a small positive voltage ($v_{DS} \approx 0.1$ volt) and gradually increase v_{GS} from zero, we will observe no drain current, i_D, until v_{GS} exceeds a certain value. This value of v_{GS} at which the drain current "turns on" is referred to as the *threshold voltage* for the device, denoted V_t*. When v_{GS} exceeds V_t sufficient charge has been distributed under the gate oxide to support drain to source conduction.

When $v_{GS} > V_t$ and v_{DS} is small, the drain current is given by the expression

$$i_D = K\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^2\right],$$

where K is a constant parameter for a given MOSFET that depends upon the width-to-length ratio of the channel and the gate oxide thickness.

If v_{DS} is kept small enough so that $(v_{DS})^2$ is negligible, i_D can be expressed as

$$i_D \approx 2K(v_{GS} - V_t)v_{DS},$$

which indicates that when $v_{GS} > V_t$ and v_{DS} is small, the channel acts like a *voltage-controlled resistor*:

* NOTE that the threshold voltage for a MOSFET, V_t, is DIFFERENT from the thermal voltage, V_T, used in the *pn*-junction equations. V_t is controlled by the design and fabrication of the MOSFET.

$$r_{DS} \equiv \frac{v_{DS}}{i_D} \approx \frac{1}{2K(v_{GS} - V_t)}.$$

The drain-to-source resistance, r_{DS}, can thus be varied by changing v_{GS}. The voltage-controlled resistance region of operation is referred to as the *triode region*, since the device behaves like a vacuum tube triode under these conditions.

These drain current equations assume that v_{DS} is very small so that $v_{GS} >> v_{DS}$, or in other words $v_{GS} \approx v_{GD}$. This assumption indicates that the channel under the oxide is essentially uniform from drain to source because the voltage difference between the gate electrode and the material under the oxide is essentially constant. We can think of this situation as a channel of constant "depth" between drain and source.

Now, if we allow v_{DS} to increase we can see that the voltage difference between the gate electrode and the channel at the source end (v_{GS}) will be *greater* than the difference between the gate electrode and the channel at the drain end (v_{GD}), since $v_{GS} - v_{GD} = v_{DS} > 0$. In this situation, we can think of the channel as being "deeper" at the source end than at the drain end, due to the varying electric field from the gate. The wedge-shaped channel has a smaller cross-section for current flow and hence a greater resistance.

If we increase v_{DS} enough, the induced channel will shrink in depth almost to zero at the drain end as soon as the voltage at the drain gets within V_t of the gate voltage (recall that the voltage difference between the gate and the channel region must be at least V_t to form a conducting channel). When this occurs the channel is said to be *pinched off*, and the drain current becomes *saturated* (constant) even as v_{DS} is increased further. The dividing line between the triode and saturation regions for *n*-channel enhancement devices is $v_{GS} = v_{DS} + V_t$: if v_{GS} is greater than $v_{DS} + V_t$ then the transistor is in the triode region; otherwise it is in the saturation region, or *off* if $v_{GS} < V_t$.

When $v_{GS} > V_t$ but $v_{GD} < Vt$, the drain current is saturated and is given by the expression

$$i_D = K(v_{GS} - V_t)^2.$$

Note that the drain current in saturation is theoretically independent of the drain-to-source voltage, v_{DS}, so the MOSFET behaves like a voltage-controlled current source when in the saturation region. The drain current in saturation is plotted as a function of v_{GS} in Figure 8.5.

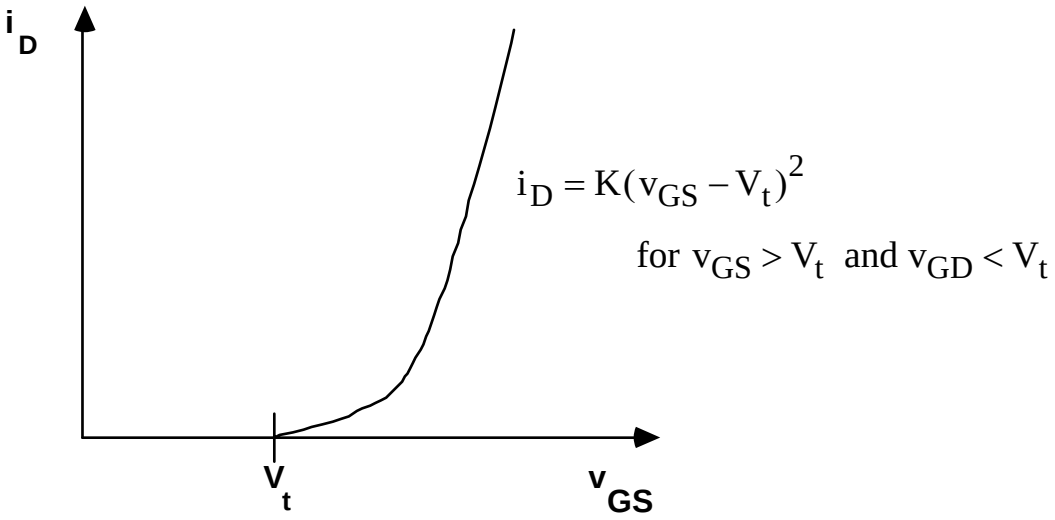


Figure 8.5

The triode and saturation characteristics are plotted in Figure 8.6.

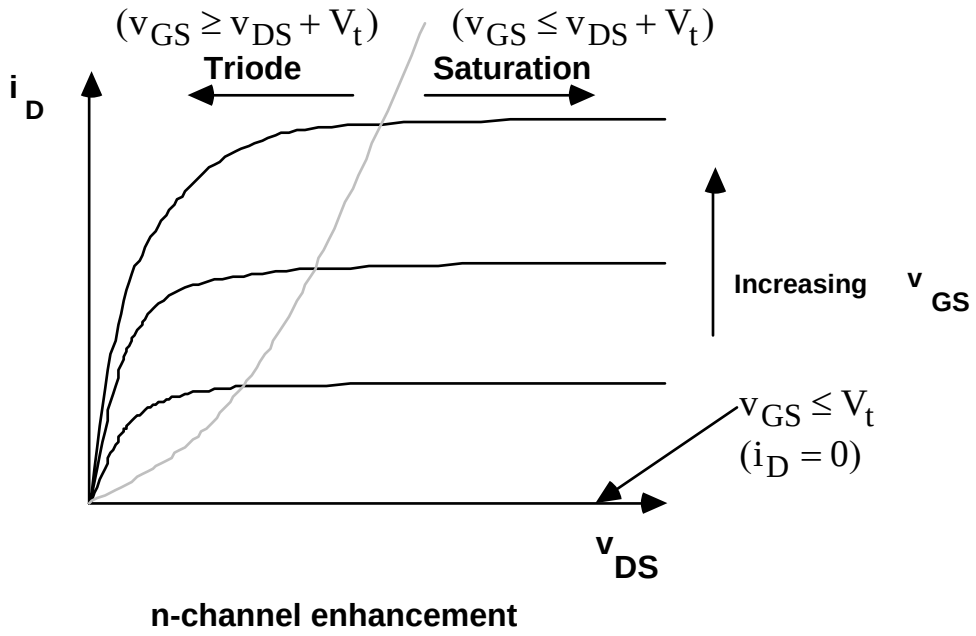


Figure 8.6

The same equations apply for the *n*-channel and *p*-channel enhancement MOSFETs if we simply define i_D to be *into* the drain for *n*-channel and *out of* the drain for *p*-channel

devices. Note that the normal operating terminal voltages differ for *n* and *p* devices. This is summarized next.

ENHANCEMENT	V_t	v_{GS}	v_{DS}	v_{GD}
n-channel	> 0	> 0	> 0	if > V_t ∅ triode if < V_t ∅ saturation
p-channel	< 0	< 0	< 0	if < V_t ∅ triode if > V_t ∅ saturation

Rather than trying to simply memorize the table, it is suggested that you keep in mind the description of the conducting channel under the various conditions since the underlying physical behavior is harder to forget than a bunch of memorized inequalities!

Channel Behavior of the Depletion MOSFET: Triode and Saturation

The behavior of depletion MOSFETs is very similar to the enhancement characteristics described in the previous section, except that the threshold voltage, V_t, is shifted to the opposite polarity. The gate voltage can either be used to deplete the the built-in channel and reduce (or stop) the flow of drain current, or the gate can be used to enhance the channel conduction just like for an enhancement MOSFET. Thus, the depletion devices can either be operated in *depletion mode* or in *enhancement mode*. The same equations apply in either case.

The drain current relationships for *n*-channel depletion MOSFETs are depicted in Figure 8.7 and Figure 8.8.

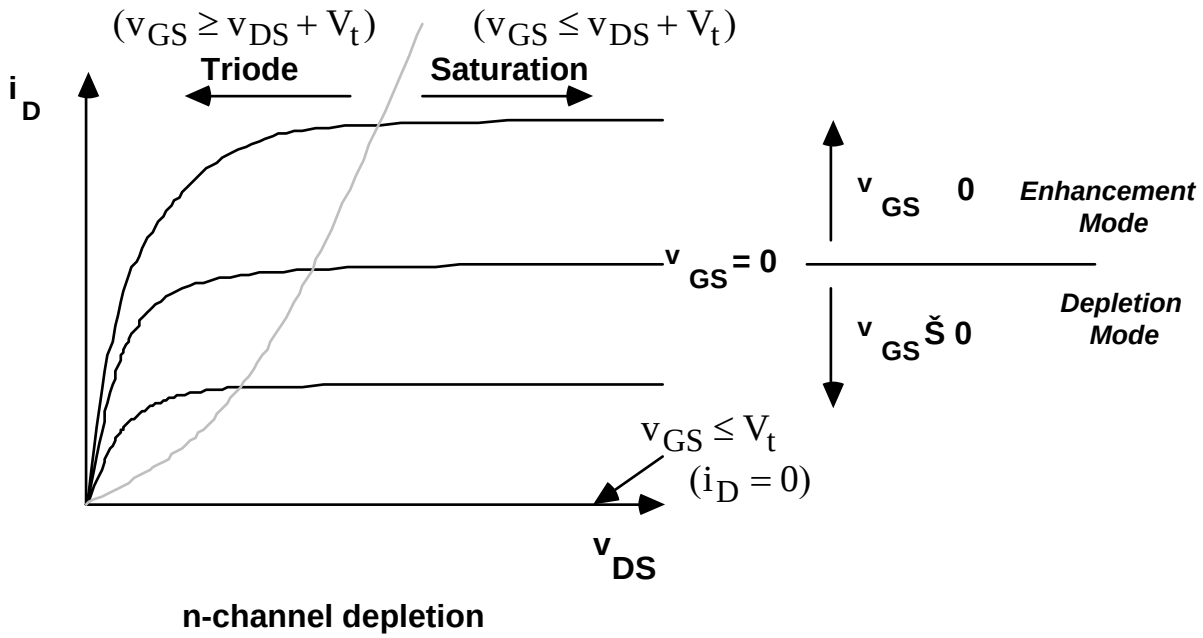


Figure 8.7

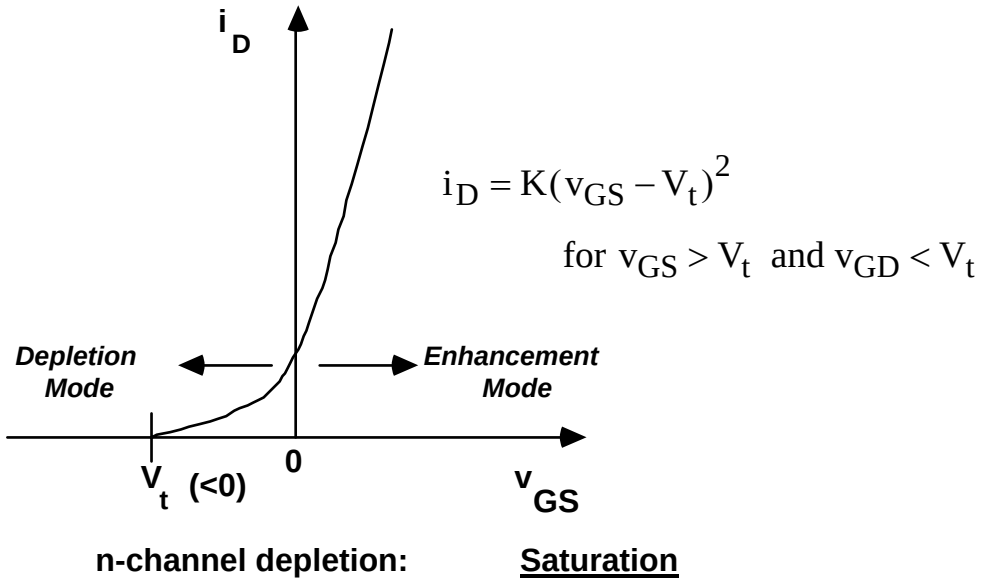


Figure 8.8

Note that in Figure 8.8 there is non-zero drain current in saturation with $v_{GS} = 0$ for depletion MOSFETs, while the drain current is zero with $v_{GS} = 0$ for enhancement devices (Figure 8.5). The depletion device saturated drain current with $v_{GS} = 0$ is denoted I_{DSS} and is given by

$$I_{DSS} \equiv i_D\big|_{v_{GS}=0,\,sat} = K(0 - V_t)^2 = KV_t^2 .$$

As with the enhancement devices, the same equations apply for the *n*-channel and *p*-channel depletion MOSFETs if we simply define i_D to be *into* the drain for *n*-channel and *out of* the drain for *p*-channel devices. Note that the normal operating terminal voltages differ for *n* and *p* devices. This is summarized below.

DEPLETION	V_t	v_{GS}	v_{DS}	v_{GD}
n-channel	< 0	> 0 ∅ enh. mode < 0 ∅ depl. mode	> 0	if > V_t ∅ triode if < V_t ∅ saturation
p-channel	> 0	< 0 ∅ enh. mode > 0 ∅ depl. mode	< 0	if < V_t ∅ triode if > V_t ∅ saturation

Another Depletion-type FET: the JFET

The first type of field-effect transistor was the *junction* FET, or JFET. JFETs make use of a *reverse biased* gate-to-channel *pn* junction instead of the gate oxide of the MOSFET devices. JFETs behave in a manner very similar to depletion MOSFETs, so the same drain current equations apply. Note, however, that JFETs are ordinarily operated only in depletion mode, since enhancement mode operation would forward bias the gate-to-channel junction.

JFETs have largely been supplanted by MOSFETs in many applications because the MOSFET offers higher input impedance due to the gate oxide. JFETs are still used in the input stages of some integrated circuit op amps fabricated with bipolar technology: the JFET provides a much higher input impedance and lower input bias currents than a BJT input stage, and JFETs can be produced directly in the same fabrication technology as the rest of the bipolar chip.

DC Analysis of MOSFET Circuits

If we wish to analyze a DC circuit containing a MOSFET it is necessary to determine whether the device is *off* (no drain current), *on* in the triode region, or *on* in the saturation region. If it is not apparent by a quick look at the circuit, we must make an assumption about the correct region of operation and then test the hypothesis. If our analysis results in a conflict with the assumption, we must try again with one of the other two possibilities. Since the saturation equation contains only I_D vs. V_{GS} (no V_{DS}

term) it is often easiest to try the saturation equation next if we can rule out the device being off.

MOSFETs for AC Small-Signal Amplifiers

BJTs are much more common than MOSFETs for use in AC small-signal amplifiers because they offer higher values of transconductance (g_m) than available from MOSFETs operated at the same DC bias current. BJTs also generally have better high frequency performance (wider bandwidth) than do MOSFETs. On the other hand, MOSFETs provide extremely high input impedance and can be operated as extremely low resistance bi-directional analog switches. MOSFETs also excel in high-power applications where voltage isolation is an advantage. Furthermore, the use of MOS devices in integrated digital circuits makes MOS the technology of choice in mixed analog and digital systems, such as A/D converters and communications switching devices. Thus, it is relevant to consider the use of MOSFETs in small-signal amplifiers.

The small-signal concept for linear amplifiers that was discussed in the preceding lab on BJTs can be applied to MOSFET circuits as well. Our approach is to bias the MOSFET in the saturation region, apply a small input signal to the gate, and approximate the nonlinear i_D vs. v_{GS} characteristic as a small, linear segment. This approach can be applied to all types of MOSFET devices. As with the BJTs, we will concentrate on a bias circuit using a negative feedback resistor in the source lead (as we did with the BJT emitter lead) to obtain bias stability.

As mentioned, the MOSFET must be biased in the saturation region in order to obtain a linear amplifier. In the saturation region we found that the drain current was related to v_{GS} according to the expression

$$i_D = K(v_{GS} - V_t)^2 .$$

If we write v_{GS} as the sum of a DC bias component (V_{GS}) and an AC small-signal component (v_{gs}),

$$i_D = K(V_{GS} - V_t + v_{gs})^2$$

$$= K\left[(V_{GS} - V_t)^2 + 2v_{gs}(V_{GS} - V_t) + v_{gs}^2\right].$$

Now, if we assume that v_{gs} is sufficiently small, v_{gs}^2 is *very* small and can be neglected. Thus,

$$\begin{aligned} i_D &\approx K(V_{GS} - V_t)^2 + 2K(V_{GS} - V_t)v_{gs} \\ &= I_D + g_m v_{gs} \end{aligned}$$

where the *transconductance*, g_m, is given by

$$g_m = 2K(V_{GS} - V_t).$$

Note that to increase the transconductance we can either increase the V_{GS} bias, or increase the value of K. Since K depends on the device geometry we will usually have to settle for bias adjustments in discrete circuits. The small-signal model for the MOSFET becomes the circuit of Figure 8.9.

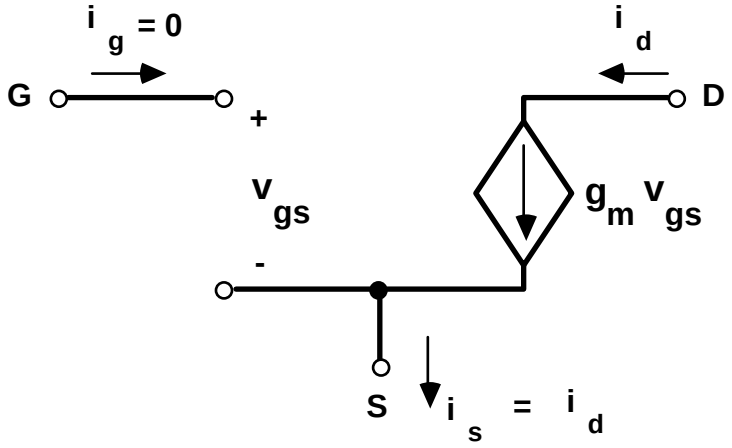


Figure 8.9

The small-signal model is similar to the BJT hybrid-π small-signal model, but notice that the gate-to-source resistance is infinite for the MOSFET. Thus, FETs are particularly useful where a high amplifier input resistance is required. Like the BJT, the MOSFET small-signal model can be made more accurate by including an output resistance, r_o, in parallel with the controlled current source. The definition of r_o is also similar to the BJT case, namely, $r_o = V_A/I_D$, where V_A is the extrapolated abscissa intercept of the drain current vs. drain-to-source voltage curves (like the Early voltage for BJTs).

Hand Analysis of MOSFET Amplifier Circuits

A hand analysis of a MOSFET amplifier circuit begins with determination of the DC bias point. The steps can be summarized:

DC ANALYSIS
• Assume the MOSFET is in the saturation region (and check this assumption later!). • Determine the DC gate voltage from the circuit, and measure or assume a value for the threshold voltage, V_t. • Calculate the DC source voltage and drain current using Ohm's Law and the saturated drain current equation. • Finally, verify that the circuit is indeed in saturation (correct relationships among the terminal voltages).

Once the DC bias conditions are calculated we can determine the small-signal parameters for the circuit, namely, g_m and r_o.

AC ANALYSIS
• Use the DC bias conditions to calculate the AC small-signal parameters: $g_m = 2K(V_{GS} - V_t), \quad r_o = \frac{V_A}{I_D}$. • Use the AC small-signal equivalent circuit (Figure 8.9) to find the input and output characteristics of the amplifier.

MOSFET Amplifier Analysis

Consider the common-source amplifier shown in Figure 8.10. An *n*-channel enhancement MOSFET is used, but a similar circuit could be constructed for any of the MOSFET types discussed earlier.

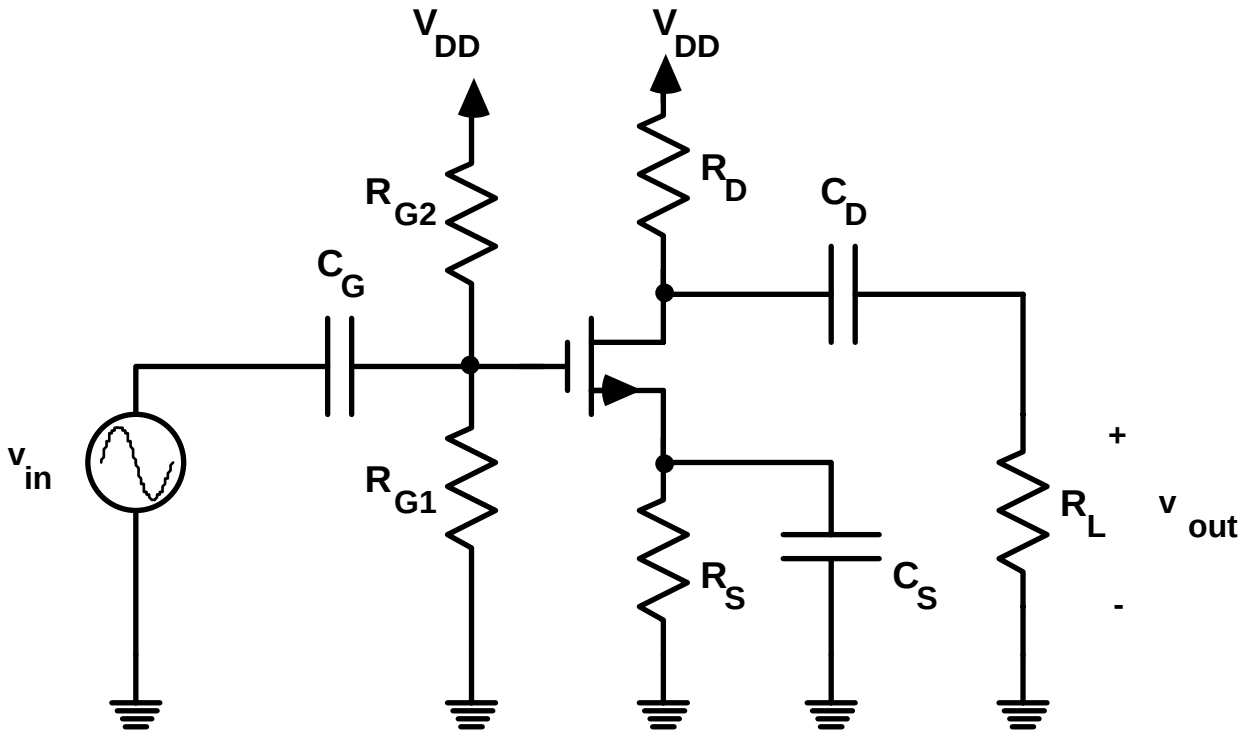


Figure 8.10

For the DC analysis we will again assume that the capacitors act like open circuits. Under these conditions the voltage at the gate is given by the voltage divider of R_{G1} and R_{G2}:

$$V_G = \frac{R_{G1}}{R_{G1} + R_{G2}} V_{DD}$$

.

If we assume that the MOSFET is in the saturation region (which it must be if we are to have a linear amplifier), the saturation drain current equation applies:

$$I_D = K(V_{GS} - V_t)^2$$

.

The two unknowns, I_D and V_{GS}, can be solved using the known value of V_G and the equation $V_S = I_D R_S$, since $V_{GS} = V_G - V_S$.

Once we have solved for I_D we need to check the MOSFET terminal voltages to make sure that the MOSFET is "on" (correct value of V_{GS} compared to V_t) and operating in the saturation region (correct value of V_{DG} compared to V_t).

The AC small-signal model for the amplifier of Figure 8.10 is shown in Figure 8.11. Note again that the capacitors are assumed to act like short circuits for the AC analysis and the DC sources are replaced by their Thévenin impedances.

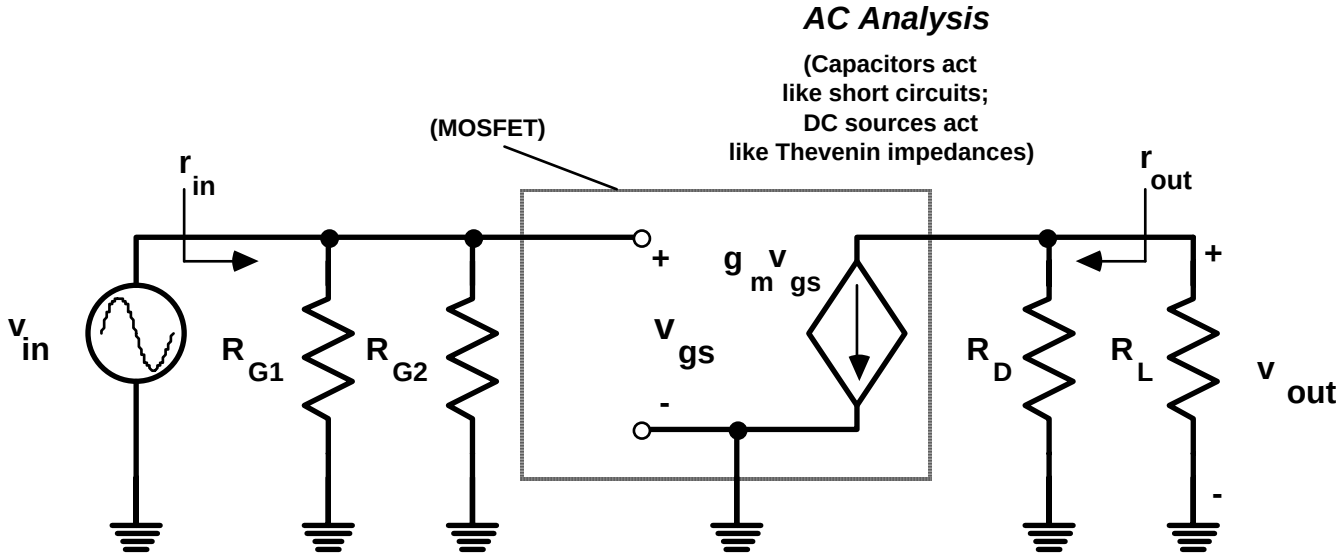


Figure 8.11

From the model we can observe several of the AC small-signal parameters for the amplifier.

- The *AC input resistance* (r_{in}) seen by the input source is simply the parallel combination of R_{G1} and R_{G2}.

- The *AC output resistance* (r_{out}) seen by the load resistor is just R_D, since the resistance of the controlled current source is infinite. Note that $r_{out} = R_D \| r_o$ if we include the non-infinite AC output resistance of the MOSFET in the model.

- The *AC small-signal voltage gain* (v_{out}/v_{in}) with the load resistor attached is given by $-g_m(R_D \| R_L)$, since $v_{gs} = v_{in}$ and the controlled current $g_m v_{gs}$ is pulled through the parallel combination of R_D and R_L in the negative direction.

MOSFETs and SPICE

Several models applicable to FETs are available using SPICE. The built-in models implement the basic triode and saturation equations, including the more complicated behavior found in actual devices. The basic SPICE format for MOSFETs is:

```
Mname   ND NG NS NB  modelname
...
.MODEL  modelname  type  (VTO=xx, KP=yy)
```

where *ND*, *NG*, *NS*, and *NB* are the node numbers connected to the drain, gate, source and substrate (body), respectively. For our purposes, the source and body should be connected together, i.e., *NS* and *NB* should be the same. The name of the MOSFET (**M***name*) is up to you, except that the first letter must be **M**, and you are also free to choose *modelname*, the name of the model. The *type* is either **NMOS** or **PMOS**.

The model parameter **VTO** is the threshold voltage for the device (V_t). Recall that V_t is positive for enhancement *n*-channel devices and negative for depletion *n*-channel devices (and vice versa for *p*-channel devices). The parameter **KP** is *twice* the parameter K used in the triode and saturation equations (**KP** = 2K)* .

The SPICE MOSFET model has other parameters and features that are used to describe the operation of MOSFETs in various configurations, frequency ranges, etc.

Discrete MOSFET Packaging

Discrete MOSFETs are typically used in relatively high power amplifier and switcher applications. Thus, the devices are usually packaged in TO-3 or TO-220 style containers for direct connection to a heat sink. *Some MOSFETs are packaged in containers with only three leads, in which case the source and substrate are usually connected together internally*. In packages with four leads the source and substrate terminals can be connected together externally if the manufacturer's data sheet indicates that this is appropriate.

* Actually, $K = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)$, while $\mathbf{KP} = \mu_n C_{ox}$. We are tacitly assuming that the width and length of the channel are the same for the simple SPICE model that is adequate for this experiment.

REFERENCES

See Chapter 5 of the text by Sedra and Smith, *Microelectronic Circuits*, 3rd ed., Saunders College Publishing (Holt, Rinehart, and Winston), 1991.

EQUIPMENT

Lab component kit (resistors, capacitors, MOSFETs)

Digital Multimeter (DMM)	Power supply	Function generator
Oscilloscope	Heathkit trainer	

PRE-LAB PREPARATION

(I) Analyze the circuits of Figure 8.12. In each case determine whether the transistor is off, in the triode region, or in the saturation region. Find the drain current and the drain, gate, and source voltages.

(II) Solid-state analog switches can be constructed using MOSFET devices. In order to be a good analog switch, the device should act like an open circuit in the "off" state, and a short circuit in the "on" state. For a real MOSFET it is not possible to obtain a perfect short circuit in the "on" state, but if the drain-to-source resistance (r_{DS}) is much smaller than the load resistance the signal loss across the device may be negligible. *Note that the MOSFET must operate in the triode region in order to obtain the required small value of "on" resistance* (the output impedance in saturation is very large). If the device enters the saturation region the current to the load saturates, meaning that the input signal no longer affects the output signal.

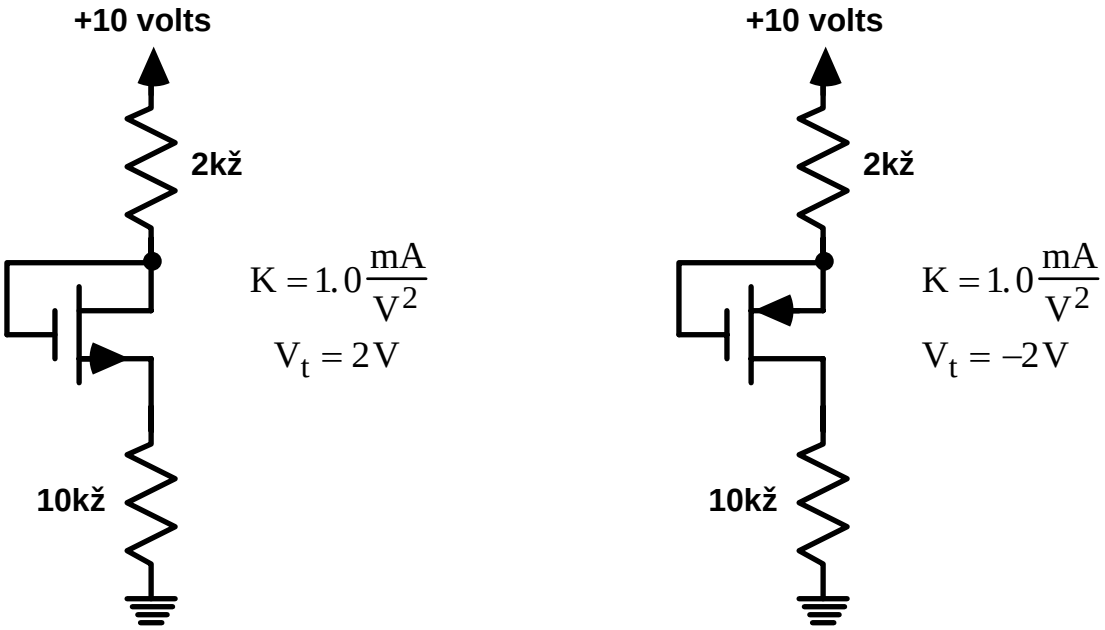


Figure 8.12

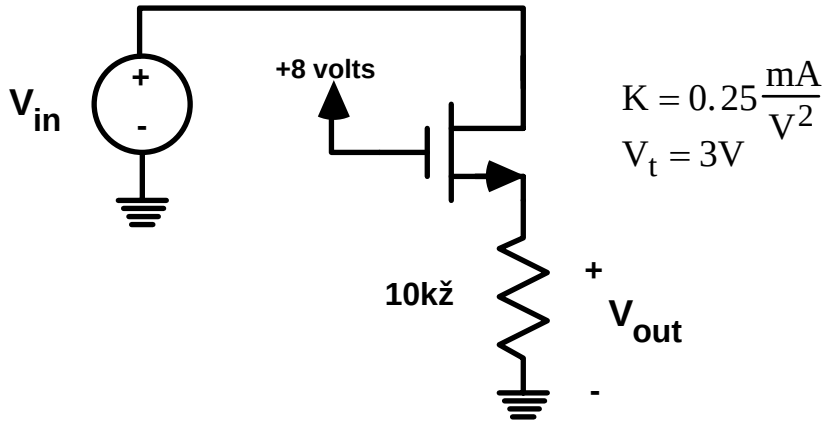


Figure 8.13

Calculate the value of r_{DS} for the switch circuit of Figure 8.13, with V_{in} = 0.1 volts. What is the voltage across the load resistor? What percent of the input signal is lost across the switch transistor? Repeat your calculations for V_{in} = 1, 2, 4, 6, and 8 volts.

Over what range of input voltage will the MOSFET in Figure 8.13 remain in the triode region?

(III) Design the *common-source* amplifier circuit of Figure 8.10 according to the following design requirements. Use SPICE to verify your design. Perform both a DC

bias analysis and an AC small-signal analysis with SPICE over the frequency range 100 Hz through 1 MHz.

- Assume V_t = 1.5 volts and K= 10 $\frac{mA}{V^2}$.
- V_{DD} = 15 volts.
- V_D (DC) ≈ 10 volts, V_G (DC) ≈ 8 volts.
- Small-signal voltage gain magnitude must be ≥ 4 in the passband (frequencies where the capacitors act like AC short circuits).
- R_L = 22kΩ.
- AC small-signal input resistance (seen by v_{in}) must be ≥ 100kΩ .
- AC small-signal output resistance (seen by R_L) must be ≤ 22kΩ.
- Assume capacitors C_G, C_D, and C_S are open circuits at DC and short circuits for AC (for SPICE, use 22μF for the capacitors).

If standard nominal resistor values (from the 5% tolerance list) are to be used, can all the specifications be met? Explain your design choices.

(IV) Using the component values you calculated in part (III), use SPICE to re-analyze the circuit assuming

(a) V_t = 1 volt, K= 2 $\frac{mA}{V^2}$, and (b) V_t = 2.5 volt, K= 0.5 $\frac{mA}{V^2}$.

Does the circuit still meet the specifications in each case?

(V) Try using the `.FOUR` statement available in PSPICE to evaluate the total harmonic distortion of your amplifier for several different input amplitudes.

EXPERIMENT

(1) Use the curve tracer instrument in the lab to obtain an I_D vs. V_{DS} characteristic for the MOSFETs in your lab kit. Use the range 0 ≤ V_{DS} ≤ 20 volts, 0 ≤ I_D ≤ 30 mA, and several steps of V_{GS}. From the curve tracer output determine the value of V_t, V_A, and K for the device (use the cursor feature of the curve tracer).

(2) Construct the analog switch circuit from Figure 8.13. Measure V_{out} and V_{DS} for $-8 \le V_{in} \le +8$ volts. Determine r_{DS} and I_D and decide whether the MOSFET is operating in the triode or saturation regions for each of your measurements.

(3) Assemble the common-source amplifier you designed in the pre-lab. *Note* that the MOSFET you use will probably have different K and V_t values than you used in your design--see what effect this has on your results and modify your design if necessary. Remember to use the proper polarity for the electrolytic capacitors! Carefully measure the DC bias conditions, then observe the output waveform for various input amplitudes and obtain an undistorted output with a 10kHz input signal Determine the AC voltage gain over the frequency range 100 Hz through 1 MHz. Try some different resistor values, different MOSFETs, etc. and observe the behavior of the circuit.

(4) Finally, experiment with some other amplifier and/or switch designs.

RESULTS

(a) (i) Present your results and calculations (V_t, K, etc.) based on the curve tracer measurements.

(ii) Since $K = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)$, estimate the W/L ratio for the MOSFET using

$\mu_n = 600\ cm^2/V \cdot sec$ (electron mobility)

and

$C_{ox} = 3.5 \times 10^{-8}\ F/cm^2$ (gate oxide capacitance per gate area).

(b) Present your measurements for the switch circuit of part 2. Give a plot of V_{out}, r_{DS}, and V_{DS} as functions of V_{in}. Indicate the range of input voltages where the MOSFET is operating in the triode region. Over what range of input voltages does the voltage drop across the MOSFET represent less than 5% of the input voltage?

(c) Describe your measurements of the common-source amplifier you designed and constructed in part 3. Did you achieve the design objectives? Did you need to modify your design in the lab to make it work? Present your voltage gain vs. frequency measurements. Describe any observations you made with different input amplitudes and resistor values. Compare your lab results with your pre-lab predictions and SPICE simulations.

(d) What other circuits did you experiment with in the lab? Did you make any further measurements and observations?

(e) How should this experiment be strengthened?

Revised 7/94

Lab # 9
TITLE: Frequency Response and Filters

ABSTRACT

This lab experiment deals with the analysis and design of frequency-dependent electrical networks. The relationship between impedance and transfer function measurements and the concept of *frequency response* is explored. Also, this lab involves the design, construction, and evaluation of some elementary filter circuits.

INTRODUCTION AND THEORY

All electrical networks and circuit elements behave differently in reaction to signals with different frequencies. This dependence upon signal frequency is commonly referred to as the *frequency response* of an electrical network. In this experiment the frequency response of several electrical networks is determined using the concepts of complex impedance from earlier in this course.

Electrical circuits can be designed to have specific frequency response characteristics. Circuits of this type are called *filters*, because they are used to *selectively* amplify or attenuate signal energy in specific frequency ranges. For example, filters are used to separate the desired frequency channel from the adjacent channels in a radio or television tuner. Another common use of filters is in audio signal processing, such as frequency equalizers, tone controls, and loudspeaker crossover networks.

Filters can either be *passive* or *active* circuits. Passive filters, as the name implies, contain only passive elements (resistors, capacitors, etc.), so they are simple to construct and economical to use. Passive filters cannot provide any power gain since they contain only passive elements. Active filters, on the other hand, include active components (transistors, op amps, etc.) and a power supply. Active filters can be designed with *negative feedback* to allow convenient component values, to diminish the effects of circuit loading, and to reduce the circuit's sensitivity to component variations. Active filters can also be used to eliminate the need for inductors, since capacitors placed in the negative feedback path create circuits with inductive properties. The elimination of inductors is particularly useful in the audio frequency range, where inductors tend to be bulky and imprecise. Inductors are also impossible to fabricate directly in integrated circuit technology.

Transfer Functions and Frequency Response

Consider the linear passive circuit of Figure 9.1. If we drive this circuit with an AC input voltage source and measure the output voltage we expect that

$$V_O(s) = H(s) \cdot V_I(s)$$

or

$$H(s) = \frac{V_O(s)}{V_I(s)}$$, where H(s) is the *voltage transfer function* of the network.

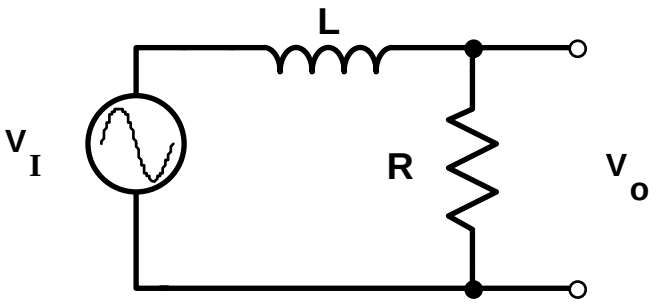


Figure 9.1

We can find H(s) by solving the network node equation:

$$\frac{V_I(s) - V_O(s)}{sL} = \frac{V_O(s)}{R}$$

yielding

$$H(s) = \frac{V_O(s)}{V_I(s)} = \frac{R}{R + sL} = \frac{R/L}{R/L + s}.$$

The transfer function can be evaluated in terms of frequency (s ∅ jω) and expressed as a magnitude and phase function — the *frequency response*:

$$|H(j\omega)| = \frac{R}{\sqrt{R^2 + (\omega L)^2}} = \frac{R/L}{\sqrt{(R/L)^2 + \omega^2}}$$

$$\angle H(j\omega) = -\tan^{-1}\left(\frac{\omega L}{R}\right).$$

It is instructive to look at the behavior for the frequency response function as the radian frequency ω varies. We can see that if **R/L >> ω** then the denominator $\sqrt{(R/L)^2 + \omega^2}$ ∅ R/L. Under this approximation |H(jω)| ∅ 1 and □H(jω) ∅ 0.

On the other hand, if **R/L << ω** then $\sqrt{(R/L)^2 + \omega^2}$ ∅ ω. In this case |H(jω)| ∝ 1/ω and □H(jω) ∅ -90°. *In other words, the circuit of Figure 9.1 behaves as a low-pass filter for voltage signals: low frequencies are passed through, while high frequencies are attenuated*. In addition to the simple low-pass filter considered above, filter circuits can be classified into four other major types: *high-pass*, *band-pass*, *band-reject* (also called *band-stop* or *notch*), and *all-pass*.

It is common in electrical engineering to define the transition point between the "passband" and the "stopband" ranges as the frequency where ω = R/L. This is the ω where the frequency response magnitude is $\frac{1}{\sqrt{2}}$ (≈ 0.707) of the passband value. Since $\frac{1}{\sqrt{2}}$ expressed in voltage dB is $20 \log_{10} (\frac{1}{\sqrt{2}}) = -3$dB, the transition point is also called the "-3dB frequency". Furthermore, because power is related to voltage squared ($P \propto V^2$), the -3dB frequency is the *half-power* frequency ($(\frac{1}{\sqrt{2}})^2 = \frac{1}{2}$).

The simple filter of Figure 9.1 is an example of a single *pole* filter. The poles of a transfer function are the denominator roots when the transfer function is expressed as the ratio of two polynomials. The denominator roots are called poles because the transfer function becomes infinite (peaks up) when the denominator contains a zero factor. In Figure 9.1, the denominator of the transfer function is (s + R/L). Thus, the transfer function has a single pole, s = -R/L.

The roots of the numerator polynomial are referred to as *zeros* of the transfer function, because a zero factor in the numerator causes the transfer function to be zero. In the Figure 9.1 example, there is no *s* in the numerator, and therefore no explicit zeros for the transfer function expression. However, the magnitude of the transfer function approaches zero as ω ∅ infinite frequency, so there is an implicit zero at infinity.

We can use a similar analysis approach for the *active* circuit of Figure 9.2.

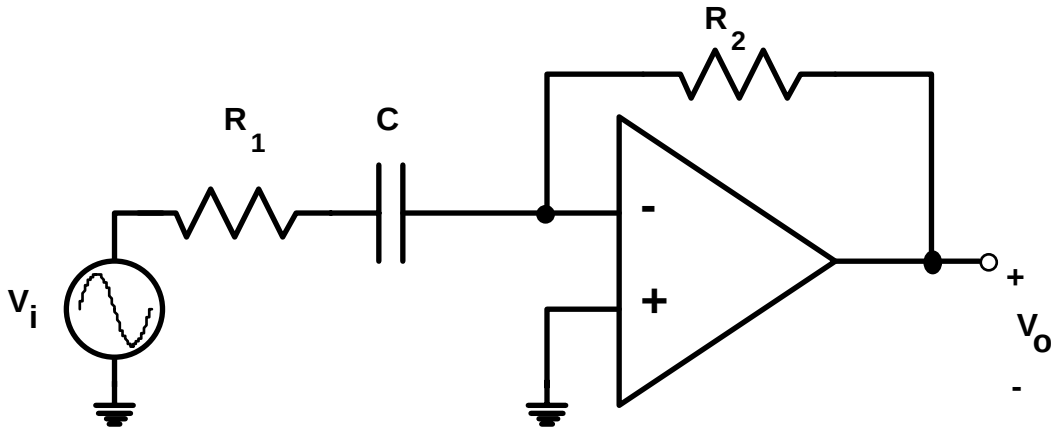


Figure 9.2

Assuming an ideal op amp,* the voltage transfer function for the circuit of Figure 9.2 is given by

$$H(s) = -\frac{Z_2}{Z_1} = -\frac{R_2}{R_1 + 1/sC} = -\frac{R_2}{R_1} \cdot \frac{s}{s + \frac{1}{R_1 C}}$$

.

This transfer function has one zero (s = 0) and one pole (s = -1/R_1C). If we consider the frequency response of this circuit (s ∅ jω) and let ω ∅ 0, we see that the low frequency response of the circuit approaches zero: the numerator goes to zero but the denominator goes to 1/R_1C. However, if we consider high frequencies (ω >> 1/R_1C) the denominator is dominated by the ω term (as is the numerator) and the response magnitude approaches -R_2/R_1. This is because the capacitor acts like an open circuit at low frequencies and a short circuit at high frequencies. Thus, the circuit of Figure 9.2 is a *high-pass* filter.

Of course, more complicated filters with more poles and zeros can be constructed using additional resistors, capacitors, and inductors. In general, the inclusion of each additional capacitor or inductor provides one additional pole and/or zero in the transfer function. The greater the number of poles and zeros, the greater the *selectivity* of the filter, meaning that the frequency response changes more drastically with frequency.

* In an actual circuit the frequency response (limited bandwidth) of the op amp itself must be considered when describing the performance of an op amp active filter.

Bode Plots

We can express an arbitrary linear transfer function as the ratio of two polynomials in *s*. If we factor the polynomials the transfer function can be expressed in the form:

$$H(s) = \frac{K_0(s - z_1)(s - z_2)\cdots(s - z_m)}{(s - p_1)(s - p_2)\cdots(s - p_n)},$$

where the z's are the zeros of the transfer function and the p's are the poles. The number of poles, n, is referred to as the *filter order*. For stability, $m \le n$. The z's and p's can be positive or negative real numbers, or even complex numbers. If we assume that the transfer function polynomials have only real coefficients then any complex zeros or poles must appear in the factored expression as *complex conjugates* (so that their product results in a *real* coefficient in the polynomial).

We are usually interested in the magnitude and phase of H(jω) as a function of frequency, ω. Expressing the magnitude and phase gives

$$|H(j\omega)| = \frac{|K_0| \cdot |(j\omega - z_1)| \cdot |(j\omega - z_2)| \cdots |(j\omega - z_m)|}{|(j\omega - p_1)| \cdot |(j\omega - p_2)| \cdots |(j\omega - p_n)|}$$

and

$$\angle H(j\omega) = \underset{(+\text{ or } -)}{\angle K_0} + \angle(j\omega - z_1) + \angle(j\omega - z_2) + \cdots \angle(j\omega - z_m) - \angle(j\omega - p_1) - \angle(j\omega - p_2) - \cdots \angle(j\omega - p_n).$$

Thus, we can obtain the frequency response magnitude and phase by determining the magnitude and phase of each zero and pole factor.

The frequency response magnitude expression can be "simplified" further if we express the function in decibel form (dB $\varnothing$ $20\log_{10}(\bullet)$):

$$20\log|H(j\omega)| = 20\log|K| + 20\log|j\omega - z_1| + 20\log|j\omega - z_2| + \cdots 20\log|j\omega - z_m| - 20\log|j\omega - p_1| - 20\log|j\omega - p_2| - \cdots 20\log|j\omega - p_n|.$$

Taking the log of the magnitude expression converts the products and quotients into sums and differences, respectively. This last expression looks bizarre, but it allows us to construct a plot of the frequency response magnitude in a very straight-forward manner. We

simply calculate the log magnitude of each zero and pole factor as a function of frequency, *then sum together the total response at each frequency*. A plot of this kind is referred to as a *Bode* (BOH-dee) plot.

The procedure is very efficient for terms where the z's or p's are *real* numbers (*simple* poles and zeros). In this case the log terms become $20\log\sqrt{\omega^2 + z^2}$. If **ω << z** then the term can be approximated as 20 log z, which is a *constant* as a function of frequency since ω does not appear. This becomes a horizontal line when plotted. Now if **ω >> z**, on the other hand, the term becomes approximately 20 log ω, which is a function that increases by +20dB for each factor of 10 increase in ω since log(10ω) = 1 + log(ω). If we plot these two approximations on semi-log paper (vertical axis is dB, horizontal axis is ω on a *log* scale), the sketch of Figure 9.3 is the result. The *straight line approximations* to the actual log magnitude function are called *asymptotes*. The sloped asymptotes are said to have a slope of ±20dB *per decade*. A similar figure applies for poles, but the sketch is flipped vertically (asymptote rolls *down* instead of up) due to the negative sign of the denominator log terms.

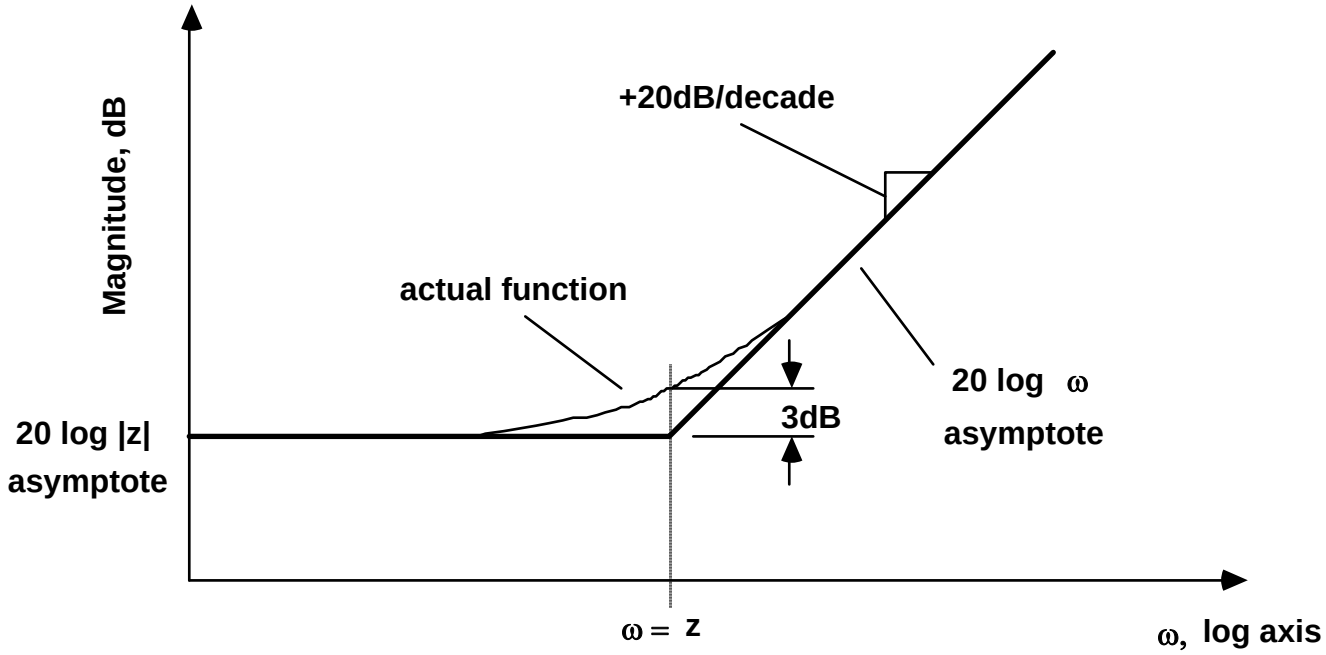


Figure 9.3

If one of the z's or p's happens to be zero then a factor (jω) will be present in the transfer function expression. The asymptote in this case is a straight line with slope

+20dB/decade (-20dB/dec for poles) which passes through 0 dB when ω = 1, since 20 log 1 = 0 dB.

The phase plot for simple poles and zeros can be developed using the same sort of approximation. The phase is given by $\angle(j\omega - z) = -\tan^{-1}\frac{\omega}{z}$. For low frequencies (ω<<|z|) the phase approaches zero (or π), while for high frequencies (ω>>|z|) the phase approaches ±π/2 (+ if z<0, - if z>0). For ω = |z| the phase is ±π/4. The usual approach to handle the phase asymptotes on the semi-log plot is to draw a straight, diagonal line starting at ϕ = 0 *one decade below* ω = |z|, and reaching ϕ = ±π/2 *one decade above* ω = |z|. The asymptote will pass through ϕ = ±π/4 when ω = |z|. This procedure is depicted in Figure 9.4 *for the case z < 0*. Note that the procedure is similar for the pole terms, except the -tan^{-1}(·) becomes +tan^{-1}(·).

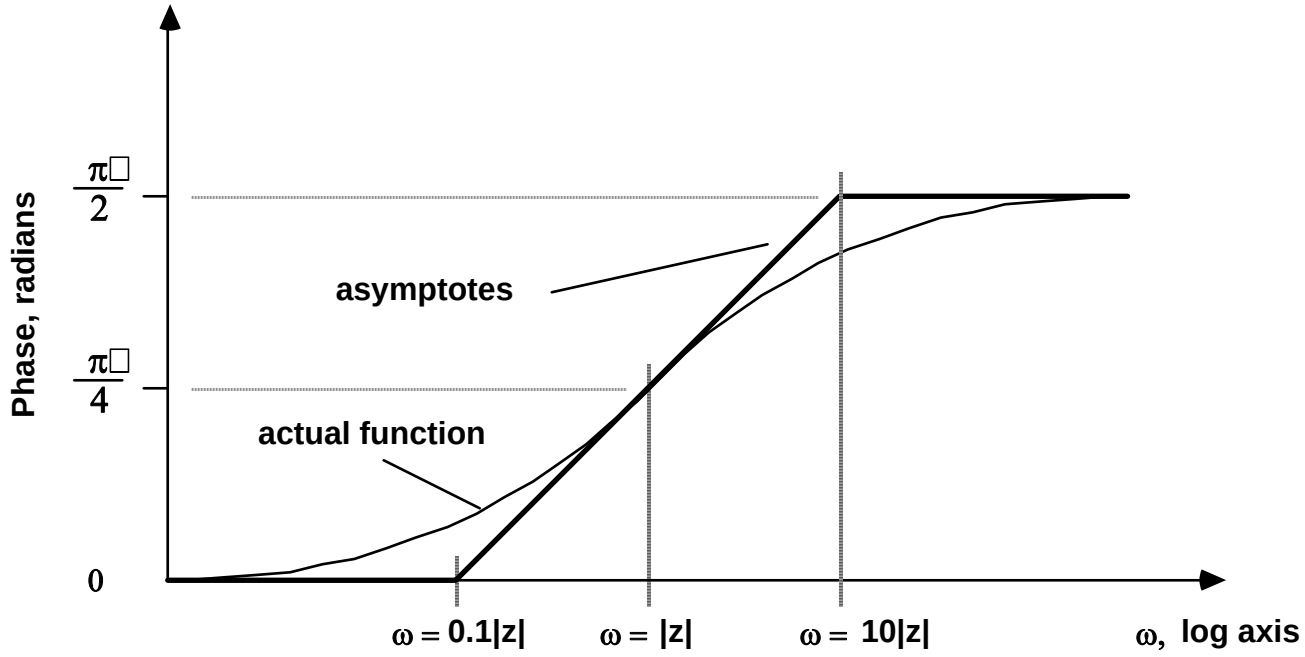


Figure 9.4

If any of the p's or z's are zero, then the phase asymptote is simply a constant +π/2 for a jω factor in the numerator or -π/2 for a jω in the denominator, since ∠(jω) = +π/2 and ∠(1/jω) = -π/2.

If p's or z's are complex numbers the usual approach is to combine the pairs of complex conjugate terms and plot the combined factor. In this case the high frequency magnitude roll up (zeros) or down (poles) occurs at twice the rate (±20dB/decade) and

the behavior in the vicinity of the breakpoint becomes "peaked". Refer to the text for more information on this procedure.

An Example of Bode Plot Methods

Consider the circuit of Figure 9.2 with R_1 = 1kΩ, R_2 = 47kΩ, and C = 0.15μF, and assuming an ideal op amp. With these component values the frequency response expression is

$$H(j\omega) = \frac{-47 \cdot j\omega}{j\omega + 6.66\overline{6}\,x10^3}$$

For the Bode magnitude plot there are three factors to consider: the constant -47 and the jω term in the numerator, and the (jω + 6.667x10$^{3)}$ term in the denominator.

Magnitude asymptotes:

(1)	20 log(47) ≈ 33.44 dB	∅	constant horizontal line at 33.44dB
(2)	20 log(jω)	∅	+20dB/dec slope (passes through 0dB @ ω=1)
(3)	-20 log(jω+6667)	∅	horizontal line at -76.48dB up to ω=6667, then -20dB/dec slope

Phase asymptotes:

(1)	□-47 = π	∅	180° (π) constant due to inversion
(2)	□jω = π/2	∅	90° (π/2) constant
(3)	□(jω+6667)$^{-1}$	∅	0 shift to ω=667, then -π/4 radians/decade slope to ω=66,667, then constant at -π/2

The Bode plot for this example constructed from the asymptotes is shown in Figure 9.5, and the frequency response obtained from a PSpice simulation is shown in Figure 9.6.

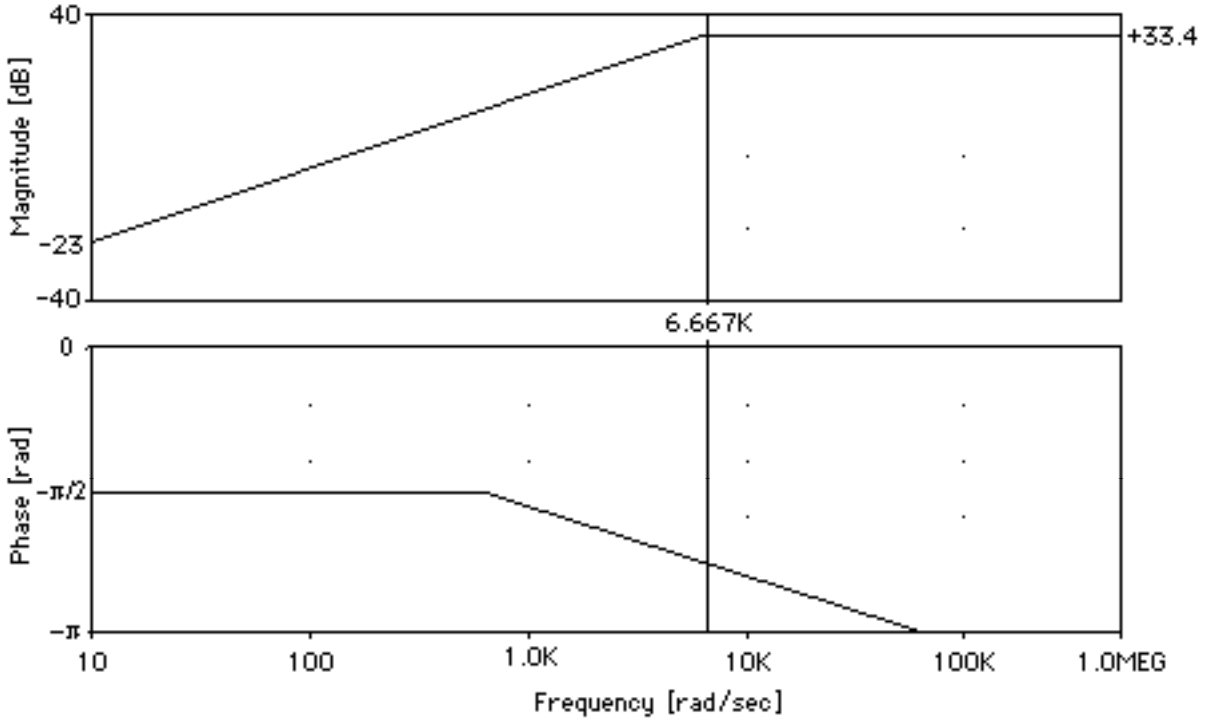


Figure 9.5

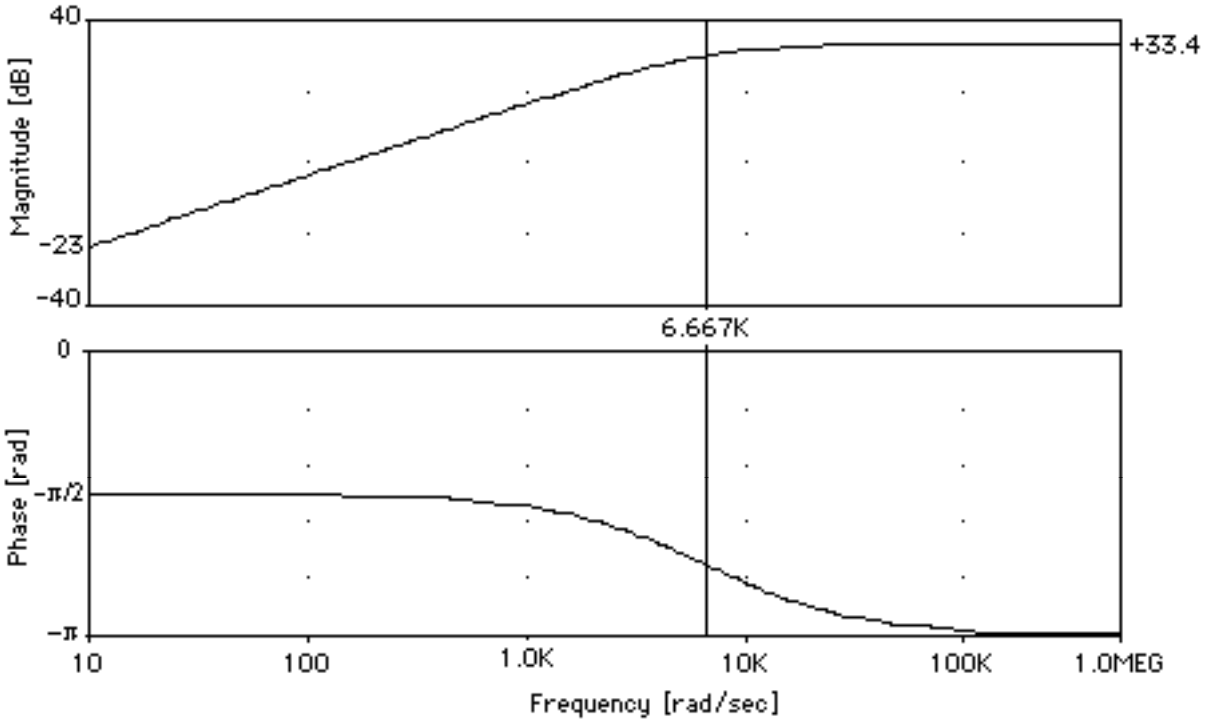


Figure 9.6

Note that although the Bode plot using asymptotes is not exactly equivalent to the true frequency response, it is still a pretty good rendition. Bode plots provide a rapid method to estimate the frequency response in terms of straight lines and breakpoints, rather than a complete point-by-point analysis.

Basic Second-Order Active Filter Functions

As mentioned previously, the order of a filter function is related to the frequency selectivity of the response: more poles and zeros result in more abrupt magnitude changes with frequency. One problem with designing highly selective filters is due to *sensitivity* of the response to small changes in component values. As the number of poles and zeros increases, so does the problem of interactions among the component tolerances and the specifications of the filter.

One way to overcome the sensitivity problem is to construct the desired high-order filter out of a combination of several low-order filters. The common approach is to connect several second-order active filters in series (called *cascade*). The active filters have very low output impedance due to the op amp structure, so there is little effect due to the loading of one stage on the next. Moreover, this reduces the overall sensitivity of the circuit by preventing variations in one stage from having any appreciable effect on the other stages.

The basic form for a second-order filter transfer function is

$$T(s) = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + (\omega_0/Q)s + {\omega_o}^2} .$$

The meaning of ω_o and Q will be discussed shortly. The two poles (roots of the denominator polynomial) of this second-order function are found by solving the quadratic equation, i.e.,

$$p_1, p_2 = -\frac{\omega_o}{2Q} \pm \frac{1}{2}\sqrt{(\omega_o/Q)^2 - 4\omega_o^2}$$

$$= -\frac{\omega_o}{2Q} \pm \frac{1}{2}\sqrt{-4\omega_o^2 \cdot \left[1 - \frac{1}{4Q^2}\right]}$$

$$= -\frac{\omega_o}{2Q} \pm j\omega_o\sqrt{1 - \frac{1}{4Q^2}}$$

The symbol ω_o is equal to the magnitude of the poles ($|p_1| = |p_2| = \sqrt{(\mathrm{Re})^2 + (\mathrm{Im})^2}$). The value of ω_o typically is near the -3dB "break" frequency in low-pass and high-pass filters and the center frequency (peak or trough location) for band-pass and band-reject filters. The Q parameter indicates the frequency selectivity of the filter: the higher the Q, the more selective the filter. Large values of Q often result in sharp peaks or troughs in the magnitude response of the filter for frequencies near ω_o. For the circuits of interest here, the value of Q will always be greater than zero, which means that the poles will always have a *negative* real part.

Note that if Q = 0.5 then 1 - $(1/4Q^2)$ is *zero*, implying $p_1 = p_2 = -\omega_o$: the two poles are real and *coincident* (equal). If Q < 0.5, then 1 - $(1/4Q^2)$ is *negative* and the square root of this quantity is imaginary, resulting in two poles which are still real, but with different values due to the "±". If Q > 0.5, on the other hand, the 1 - $(1/4Q^2)$ argument is *positive*, giving two poles that are *complex conjugates*.

The roots of the numerator of the T(s) expression (the zeros) indicate the overall shape of the transfer function. The zeros can be complex numbers, but they are often chosen to be purely imaginary so that complete attenuation is achieved at certain frequencies (such as DC for a low-pass filter).

In short, the denominator (poles) of T(s) gives information about *where* in frequency any breakpoints, peaks, dips, etc. occur in the frequency response, while the numerator (zeros) of T(s) indicates the *type* of filter response (low-pass, high-pass, etc.).

Some Filter Design Concepts

In most engineering situations we are given a filter description in the form of several performance requirements, rather than directly in the form of poles, zeros, Q, etc.

Performance requirements for the magnitude response usually involve the specification of:

- Range of frequencies for the passband (-3dB bandwidth)
- Range of frequencies for the stopband
- Nominal gain and ripple in the passband
- Nominal attenuation in the stopband

These specifications are depicted in Figure 9.7 for an example low-pass response. Note that a *transition* band is present between the passband and stopband frequency ranges. The magnitude *ripple* refers to the peak-to-peak deviation from the nominal gain value. Ripple usually refers to a nonmonotonic magnitude characteristic in which the gain decreases *and* increases with frequency across the passband. Also, be aware that additional specifications on the phase behavior of the filter may be included for some applications.

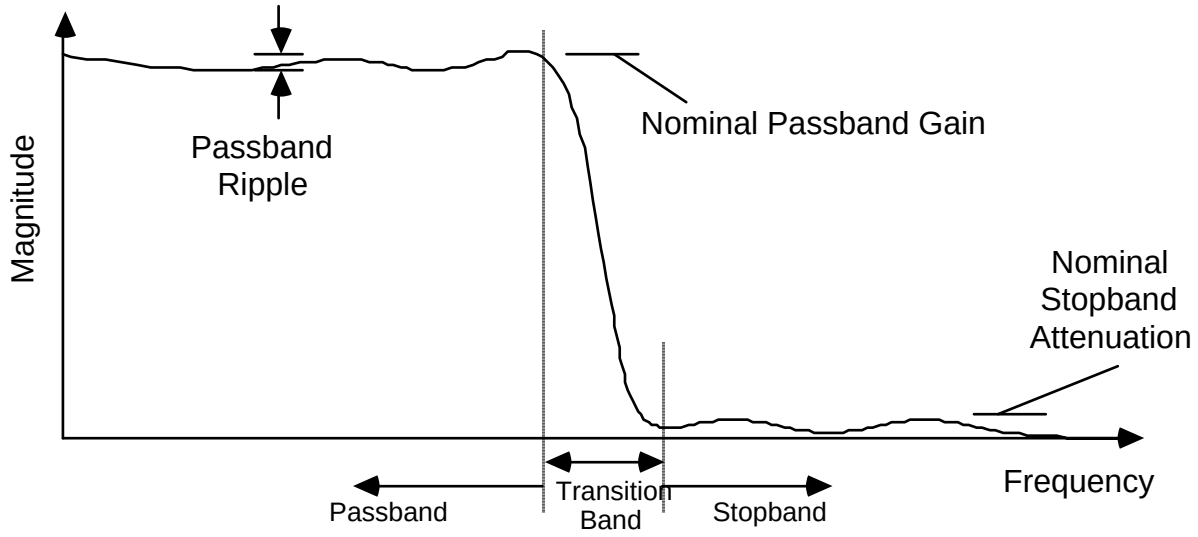


Figure 9.7

Entire textbooks are written on methods to choose transfer functions which meet or exceed a given set of performance specifications, so we certainly won't attempt to cover the entire range of possibilities. In practice, a specific class of transfer functions with known properties is often chosen first, then the required parameters to achieve the performance requirements are obtained from a table of design values. An example of this procedure will be considered later.

Once we have determined the desired transfer function we must somehow come up with a circuit that will implement it. As with the choice of transfer function, the choice of circuit topology is the subject of numerous books and journal articles. Filter network

design typically involves a tradeoff among many competing criteria, e.g., number and cost of components, sensitivity of the circuit to component variations, ease of manufacturing, and so forth. The practical approach in all but the most demanding situations usually involves the selection of a few reasonable circuit configurations for evaluation and comparison.

An Example Filter Design

To complete this brief introduction we will consider the design of a second-order low-pass active filter. The design of more complicated filter networks will be considered in other courses, but the basic procedures are similar.

Problem: An input signal to an amplifier is contaminated with noise energy at 15.75kHz and above due to a television monitor near the amplifier (the 15.75kHz signal is the horizontal scanning frequency of the TV display). We would like to use a second-order (for simplicity) low-pass active filter to attenuate frequencies above and including the 15.75kHz range by at least 50dB compared to the nominal passband gain of unity, and no ripple is allowed in the passband. What is the available -3dB bandwidth for the passband?

The situation can be depicted in the form of a Bode plot, as shown in Figure 9.8.

It can be shown that one way to achieve the requirement of no ripple in the passband is to define a filter whose magnitude response is *maximally flat*, meaning that the first *n-1* derivatives of the magnitude function are zero at $\omega=0$. A maximally flat response filter is referred to as a *Butterworth* filter, named for a British engineer.

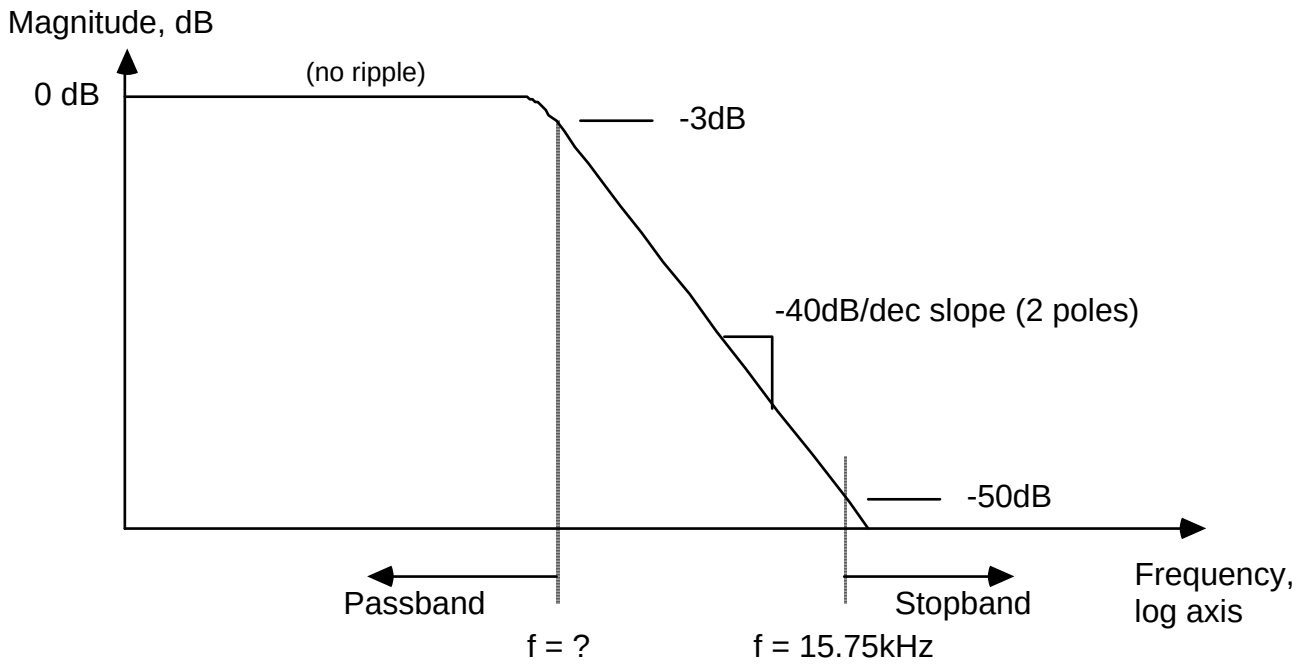


Figure 9.8

The general second-order Butterworth low-pass transfer function, H(s), is given by

$$H(s) = \frac{K_o\,\omega_o^{\,2}}{s^2 + \sqrt{2}\cdot\omega_o s + \omega_o^{\,2}}$$, where we can see that $Q = 1/\sqrt{2}$.

The general Butterworth low-pass *magnitude* function can be written as

$$\left|H(j\omega)\right|_{\text{Butterworth}} = \frac{K_o}{\sqrt{1+\left(\frac{\omega}{\omega_o}\right)^{2n}}}$$, where n is the filter order and ω_o is the -3dB frequency,

and the second-order form for this example (n=2, K_o = 1) is

$$\left|H(j\omega)\right|_{\text{Butterworth}} = \frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_o}\right)^{4}}} = \frac{1}{\sqrt{1+\left(\frac{f}{f_o}\right)^{4}}}$$.

Since we require that $|H(j\omega)| \le$ -50dB (3.162×10^{-3}) when f = 15.75kHz, we can use the magnitude expression to solve for the -3dB frequency f_o:

$$3.162\text{x}10^{-3} = \frac{1}{\sqrt{1+\left(\frac{15.75\text{kHz}}{f_o}\right)^4}},$$

giving f_o = 886 Hz. Thus, in order to meet the specifications with a second-order Butterworth filter we have a -3dB bandwidth of 886 Hz.

Now, in order to implement this active filter we need a circuit that has the transfer function

$$T(s) = \frac{(2\pi\cdot 886)^2}{s^2 + \sqrt{2}\cdot(2\pi\cdot 886)s + (2\pi\cdot 886)^2}.$$

A prototype circuit is shown in Figure 9.9. This particular configuration is known as a *Sallen-Key* filter, named for the two originators. The op amp is connected in a unity gain configuration, so v_o must be equal to the voltage across C_1. Note that at very low frequencies the capacitors act like open circuits and $v_o = v_i$, while at very high frequencies the capacitors "short-out" and v_o goes to zero. The transfer function ($V_o(s)/V_i(s)$) of the circuit is found to be:

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1+(R_1+R_2)C_1\cdot s + R_1R_2C_1C_2\cdot s^2}$$

$$= \frac{\frac{1}{R_1R_2C_1C_2}}{s^2 + \frac{R_1+R_2}{R_1R_2C_2}\cdot s + \frac{1}{R_1R_2C_1C_2}}$$

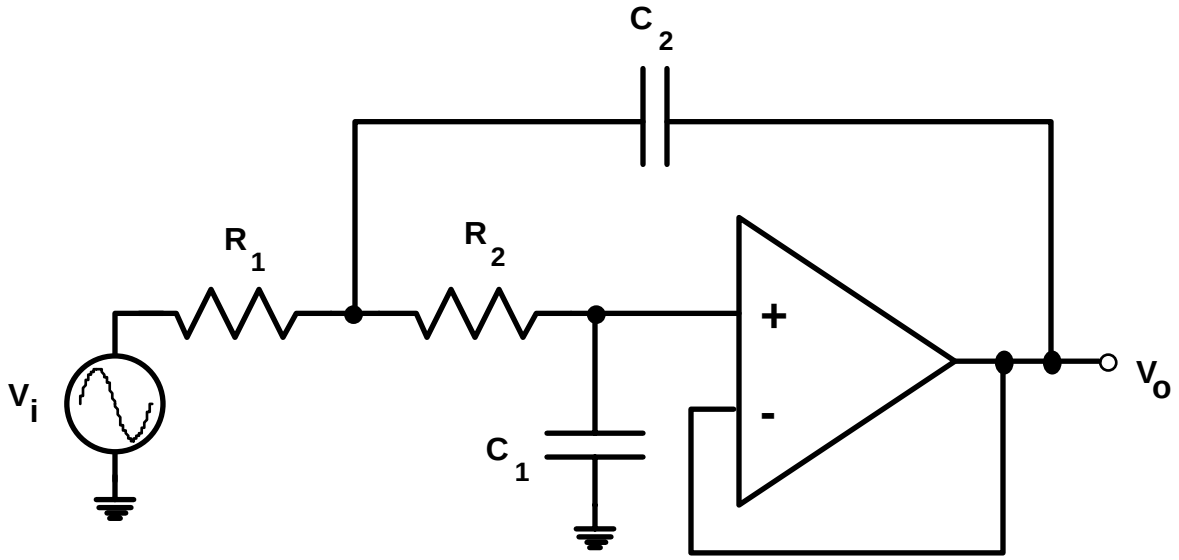


Figure 9.9

If we compare this last expression to the desired transfer function for our filter (see T(s) above), we see that the prototype filter will implement the desired function if we choose the components so that:

$$\frac{1}{R_1 R_2 C_1 C_2} = \omega_o{}^2 = (2\pi \cdot 886)^2$$

and

$$\frac{R_1 + R_2}{R_1 R_2 C_2} = \frac{\omega_o}{Q} = \sqrt{2} \cdot 2\pi \cdot 886 \quad .$$

These two design equations have four unknowns (R_1, R_2, C_1, and C_2) so we will be able to choose some of the unconstrained values. For example, if we *arbitrarily* choose **$R_1 = R_2 = R$ and let $C_1 = \alpha C_2 = \alpha C$**, the design equations become

$$\frac{1}{\alpha (RC)^2} = (2\pi \cdot 886)^2 \quad \text{and} \quad \frac{2R}{R^2 C} = \frac{2}{RC} = \sqrt{2} \cdot 2\pi \cdot 886 \quad .$$

Solving these equations for **α** and the product **R C** gives

$$\alpha = \frac{1}{2} \text{ and } \quad RC = \frac{\sqrt{2}}{\omega_o} = \frac{1}{\sqrt{2} \cdot \pi \cdot 886} \approx 2.54 \times 10^{-4} \quad .$$

Now in order to implement the design we can try a range of "convenient" values for the components, say, resistors from the 5% tolerance list and capacitors in the 0.01μF to 1μF range. *Note that this will result in an approximation to the theoretical response!* One possible combination is

$$R_1 = R_2 = R = 12k\Omega$$
$$C_2 = C = 0.022\mu F$$
$$C_1 = \frac{1}{2} C_2 \approx 0.01\mu F$$

Finally, we should compare the response using this combination of components to the theoretical transfer function. In a practical situation we should also consider the sensitivity of the circuit's performance due to component tolerance variations.

REFERENCES

For basic frequency response concepts, see Chapter 14 of the text by J. David Irwin, *Basic Engineering Circuit Analysis*, 4th ed., Macmillan Publishing Co., 1993.

For basic filter topics, see Chapters 7 and 11 of the text by Sedra and Smith, *Microelectronic Circuits*, 3rd ed., Saunders College Publishing (Holt, Rinehart, and Winston), 1991.

For more comprehensive treatment of active filters, see the engineering library under the search subject: `ELECTRIC FILTERS ACTIVE`.

EQUIPMENT

Lab component kit	Multimeter	LC meter
Function generator	Oscilloscope	Heathkit trainer

PRE-LAB PREPARATION

(I) Determine the transfer function of the circuit of Figure 9.10 below, using R = 1kΩ, L = 0.1 H, and C = 0.22μF. What are the poles and zeros? Plot the magnitude and phase response of the circuit in Bode form (asymptotes) Indicate all slopes and breakpoints. Is the response low-pass or high-pass? What is the -3dB frequency?

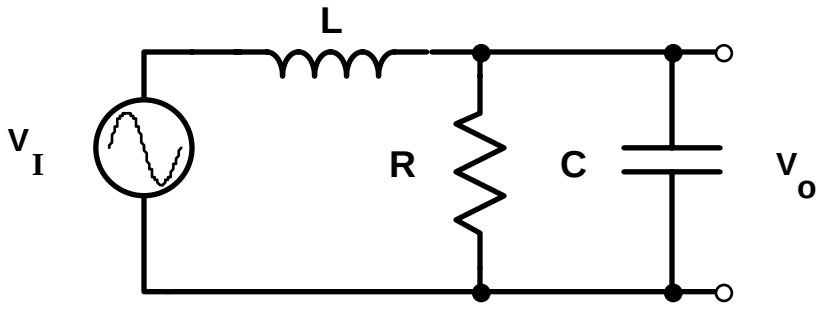


Figure 9.10

(II) Determine and plot the transfer function of the active filter circuit shown in Figure 9.11. Estimate ω_o and Q in terms of the circuit components.

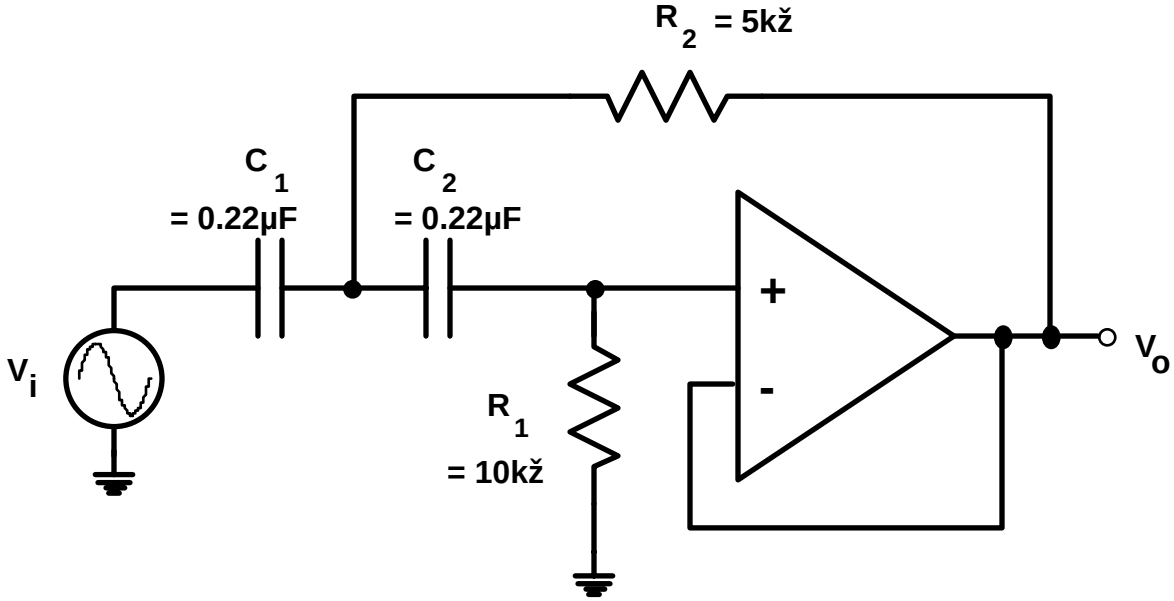


Figure 9.11

(III) The Butterworth low-pass filter designed in the introduction has a maximally-flat magnitude response (no ripple). We can obtain a somewhat more abrupt transition at the passband edge if we can tolerate some ripple in the passband. One transfer function of this type is referred to as the *Chebyshev* response, since the denominator involves Chebyshev polynomials. The Chebyshev response has the characteristic that all the ripples in the passband have the same amplitude. An example of a Chebyshev transfer function is:

$$T(s) = \frac{0.707948\,\omega_b{}^2}{s^2 + 0.64490\,\omega_b s + 0.707948\,\omega_b{}^2},$$

where ω_b is the frequency where $|T(j\omega)|$ drops -3dB below the peak gain. This particular Chebyshev transfer function allows a 3dB ripple amplitude in the passband.

T(s) can be rewritten in the form of ω_o and Q as

$$T(s) = \frac{\omega_o{}^2}{s^2 + 0.76646\,\omega_o s + \omega_o{}^2}$$

where $\omega_o = \sqrt{0.707948} \cdot \omega_b$, and $Q = 1.3047 = \sqrt{0.707948}/0.64490$. Note that the -3dB frequency (ω_b) is *not* equal to ω_o for the Chebyshev filter.

(i) Let ω_b = 1 rad/sec and plot $|T(j\omega)|$ for $0.01 \le \omega < 100$. Use a computer to generate the plot, if you wish.

(ii) Using the Sallen-Key filter circuit of Figure 9.9, design a Chebyshev low-pass filter to meet the gain specifications required in the filter design example worked in the introduction: the gain magnitude of the filter at 15.75kHz must be -50dB. Give the desired value of ω_b and your choice of nominal component values.

Note that

$$|T(j\omega)| = \frac{1}{\sqrt{1 - 1.4125\left(\frac{\omega}{\omega_o}\right)^2 + \left(\frac{\omega}{\omega_o}\right)^4}}$$

(iii) Use PSpice to generate Bode plots (magnitude and phase) for the Butterworth design (pre-lab) and your Chebyshev design. Use an ideal (voltage-controlled voltage source) op amp model.

EXPERIMENT

NOTE: you may need or want to use combinations of the components in your lab kit to obtain the required resistance values.

(1) Assemble RLC ladder network of Figure 9.10 using the nominal components R = 1kΩ, L = 0.1 H, and C = 0.22μF, as in the pre-lab. Measure the actual component values used. Measure the magnitude and phase response of the network and compare to your expectations (plot the results in Bode form).

(2) Assemble the RC active filter circuit of Figure 9.11. Measure the magnitude and phase response of the circuit keeping in mind your results from the pre-lab.

(3) Now assemble and evaluate the Sallen-Key Chebyshev filter you designed in the pre-lab. Carefully measure the gain and phase response, noting any discrepancies from the expected performance. Also, observe and sketch the output waveform when a square wave input signal of various frequencies is applied to the circuit.

RESULTS

(a) Present your measurements of the RLC passive filter from part 1. Explain your measurements and compare the actual results to your predictions from the pre-lab. What are the factors that account for any differences?

(b) Explain your measured results for the RC active filter considered in part 2 of the experiment. Did the frequency response match your expectations? What effect does the op amp (non-ideal) have on the filter response at high frequencies?

(c) How did your Chebyshev filter perform when you built it? Did the non-exact component values affect the response? Present your measured frequency response gain and phase, and your square wave output sketches. Explain the significant features.

(d) Give some examples of improvements that should be made to this experiment.

Revised 7/94

Lab #10
TITLE: Power Relationships and Power Factor

ABSTRACT

Electrical power is a measure of the rate at which energy is transferred from place to place in an electrical network. This experiment involves measurement of power in circuits containing both resistive (dissipative) and reactive (energy storage) elements. The relationships among the terms instantaneous power, average power, RMS or effective power, apparent power, and complex power are considered in mathematical and practical terms. Calculation and correction of the power factor of an electrical load are also investigated.

INTRODUCTION AND THEORY

In a DC circuit, power is measured by determining the voltage, current and/or resistance and using a suitable form of V*I=P. The same method could also be used to measure power in a AC circuit but is not because there is an additional variable (power factor) involved which affects the price at which the power company can deliver power to your house (or factory or farm). Large industrial loads (usually large motors) cause the PF to be lower than the ideal value of 1. If the load has a low PF, lines running to the plant will be forced to carry a higher current (I_{RMS}). Since line losses are proportional to I_{RMS}^2, the power company will be forced to generate more total power to furnish the same power to the plant. The power company will charge more for a load with a low PF or the plant must purchase and install large capacitors to raise the PF.

RMS voltages and currents are used when discussing ac power so that the *effectiveness* of each source in delivering power to a resistive load can be compared. The effective value of DC is the DC value. Sinusoidal voltages/currents are converted to RMS by dividing by $\sqrt{2}$. While sinusoidal waveforms are the most common type of ac (all house wiring), other ac waveforms are also used, such as half or full-wave rectified sinusoidal, square wave, triangular, or ramp. Each can be converted to RMS by multiplying by a (different) constant.

REFERENCES

See chapter 11 of the text by J. David Irwin, *Basic Engineering Circuit Analysis*, 4th ed., Macmillan Publishing Co., 1993.

EQUIPMENT

Lab component kit
Signal Generator
Heathkit Trainer (or breadboard)
0.1 H inductor
Multimeter (RMS)
Oscilloscope

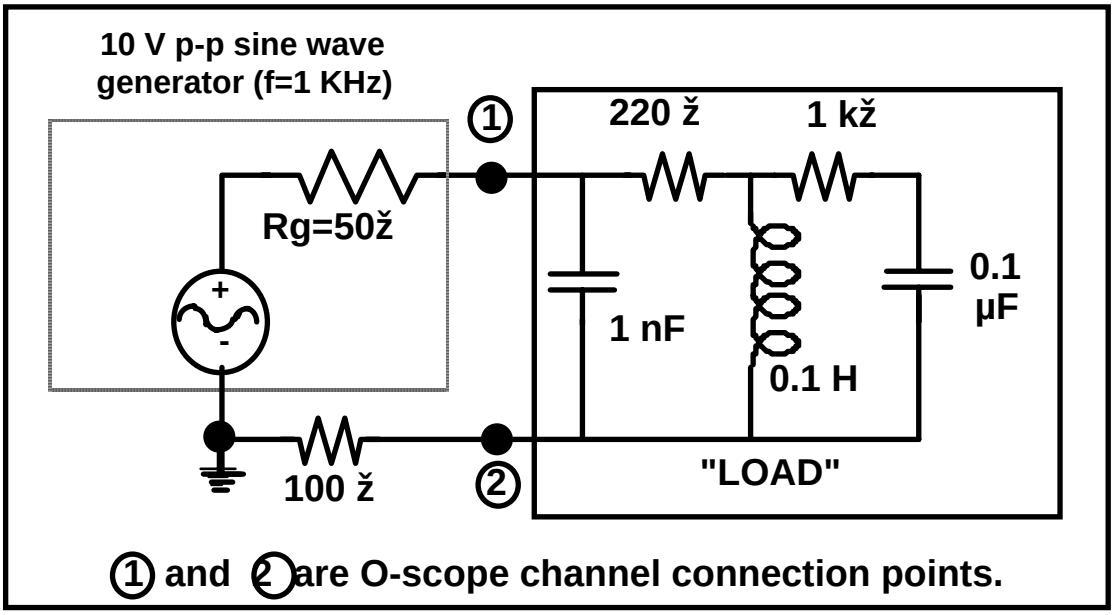


Figure 10.1

PRE-LAB PREPARATION

(I) Consider the circuit of Figure 10.1.

(a) Calculate the impedance (Z_L) of the "load".
(b) Given $V_{G(M)}$ (maximum sine generator voltage)= 5∅0° V, calculate the phasor current (I), $V_{R\ (M)}$ (maximum voltage across the 100 Ω resistor), $V_{L(M)}$ (maximum load voltage), and PF (load power factor).

(II) Assume you used a multimeter (which reads RMS voltage) to obtain the **RMS** voltages for V_G, V_R, and V_L. Convert the calculated (maximum) values from part (I) to RMS values and use a phasor diagram to **graphically** determine the PF.

(III) Calculate the apparent power, average power, and reactive power for the load.

(IV) Calculate the capacitance which, when placed in parallel with the load, will raise the PF to 1.

(V) Use SPICE to determine the PF of the (original) load. Determine the phase difference between the load voltage and current. Now include the capacitor (part IV) and determine the new PF.

EXPERIMENT

(1) Use the inductance/capacitance meter to measure the exact component values for the inductor and capacitors used in this experiment. Also measure the ESR (equivalent series resistance) of the capacitors). Use a multimeter to measure the exact values for the resistors used.

(2) Use the oscilloscope to measure the phase angle between the load voltage and current (measured through the 100Ω resistor). Connect the O-scope and circuit as in Figure 10.1. **NOTE: Since the signal generator and 'scope are both internally grounded to the power line, measuring the phase angle between the load voltage and the current is <u>not</u> straightforward**. One method is to:

i) Connect channels 1 and 2 as shown. Set ch1 to be the trigger, and set the *same* vertical amplification for each channel. (Now "ch1-ch2" is the load voltage and "ch2/100Ω" is the load current).

ii) Observe ch2 and adjust so a positive slope zero crossing aligns with a graticule (line on the 'scope face).

iii) Switch to **ADD** mode (with ch2 inverted) to get the load voltage signal.
iv) Measure phase shift by measuring the time shift between positive zero crossings of "ch1-ch2" and "ch2" (the screen graticule set in part ii).
v) Make sure the waveforms are centered about the zero-volt axis (they tend to shift when going to/from the "ch1-ch2" mode

Use the (RMS) multimeter to measure the voltages across the load, generator, and the 100 Ω "current measuring" resistor.

Use the measured phase angle and the RMS voltage/current from the meter to calculate (a) PF, (b) apparent power, (c) average power, (d) reactive power, and (e) complex power

(3) (a) Calculate the capacitance needed to raise the PF to 1.
(b) Connect the calculated capacitance (from a), re-adjust the signal generator to 10 V p-p, and again measure the phase angle between the load voltage and current.
(c) Again use the RMS multimeter to measure the voltages across the load, generator, and the 100 Ω resistor (as in part 2).

Repeat the power calculations of step 2.

RESULTS

(a) Compare the PF determined 1) analytically (pre-lab I), 2) graphically (pre-lab II), 3) with SPICE (pre-lab V), 4) with the 'scope in the lab. Discuss any variations in results.

(b) Compare apparent power, average power, and reactive power results from the pre-lab and experiment. Did power supplied by the generator or power consumed by the load change? Compare the current magnitudes at the different power factors. Discuss any significant variations in results.

(c) Discuss some of the economic considerations of the power factor, from the viewpoint of the power company and from the viewpoint of a large industrial power consumer.

(d) What can be done to improve this experiment?

Revised 7/94

Lab # 11
TITLE: Transformers

ABSTRACT

The characteristics of a small power transformer are compared to *ideal* and *first-order* transformer models. Measurements of transformer parameters and transformer applications are also examined, including a simple, unregulated DC power supply.

INTRODUCTION AND THEORY

A transformer is a four-terminal device in which AC complex power is applied at one pair of terminals (the *primary*) and a load is driven at the other pair of terminals (the *secondary*). The transformer is a magnetically coupled device with no direct electrical connection between the primary and the secondary windings, so no DC power can pass through the device. The behavior of an actual transformer is rather complicated, but several simplified models are available for analyzing basic transformer circuits.

The Ideal Transformer Model

An ideal transformer is lossless, meaning that the complex output power at the load is equal to the complex input power. A simple diagram representing the ideal transformer is shown in Figure 11.1.

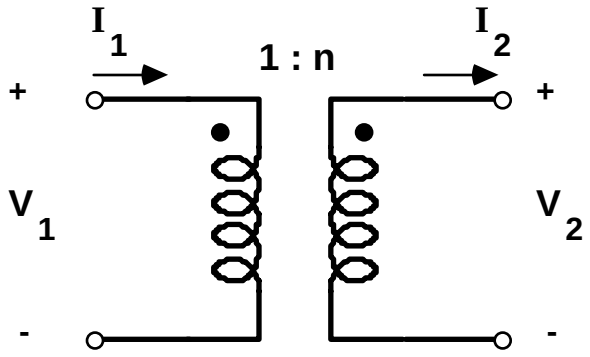


Figure 11.1

The ideal transformer can either *step up* or *step down* the AC output voltage ($\mathbf{V_2}$) with respect to the input voltage ($\mathbf{V_1}$) in order to obtain the desired voltage level at the load. Since no power is lost in the ideal transformer, stepping up the output voltage by a factor n results in $\mathbf{V_2} = n\,\mathbf{V_1}$, and $\mathbf{I_2} = \mathbf{I_1}/n$, where n is the *turns ratio* of the transformer,

i.e., [# of turns in secondary winding]/[# of turns in primary winding]. The dots (•) at the top of the diagram in Figure 11.1 are used to indicate the polarity of the windings: a positive AC voltage $\mathbf{V_1}$ results in a positive AC voltage $\mathbf{V_2}$.*

The typical application of transformers is depicted in Figure 11.2. In this example a sinusoidal source drives the primary and a load impedance is attached to the secondary.

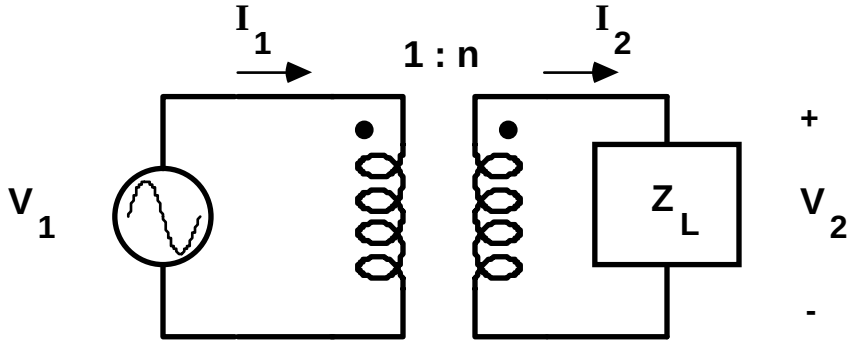


Figure 11.2

If we assume that the transformer is ideal we can identify the complex (phasor) expressions which relate the terminal voltages and currents.

$$n\mathbf{V_1} = \mathbf{V_2} \qquad \mathbf{I_1}/n = \mathbf{I_2} \qquad \mathbf{V_2}/\mathbf{I_2} = \mathbf{Z_L}$$

Using these expressions we can also write

$$\mathbf{Z_1} = \frac{\mathbf{V_1}}{\mathbf{I_1}} = \frac{\mathbf{V_2}/n}{n\mathbf{I_2}}$$

$$= \frac{\mathbf{1}}{n^2} \cdot \mathbf{Z_L}$$

This result indicates that for an ideal transformer the input impedance seen at the primary is equal to the impedance attached to the secondary divided by the square of the turns ratio. An equivalent circuit corresponding to this relationship is shown in Figure 11.3. It is also possible to determine the output impedance of this ideal

* If the primary and secondary currents both flow into or out of the dotted terminals, the induced magnetic fluxes *add*. For this reason, NOTE that while the winding current is shown as *in* for the primary and *out* for the secondary in Figure 9.1, you may find that some other textbooks and references define both currents as flowing *in*.

transformer circuit (impedance seen by the load), which is n^2 times the source impedance. If an ideal voltage source is assumed, then the output impedance is zero.

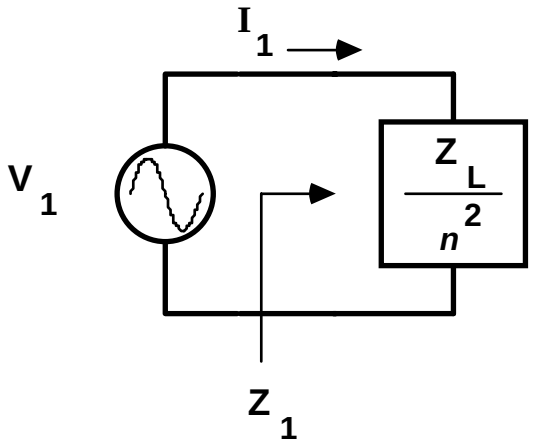


Figure 11.3

The impedance transformation relationship is interesting because it allows a transformer to be used in matching the impedance from one circuit to another.

A First-Order Low-Frequency Model

An actual transformer differs from the ideal model primarily due to the resistance and inductance of the windings and the incomplete coupling of magnetic flux between the primary and secondary windings. A model incorporating these effects is given in Figure 11.4

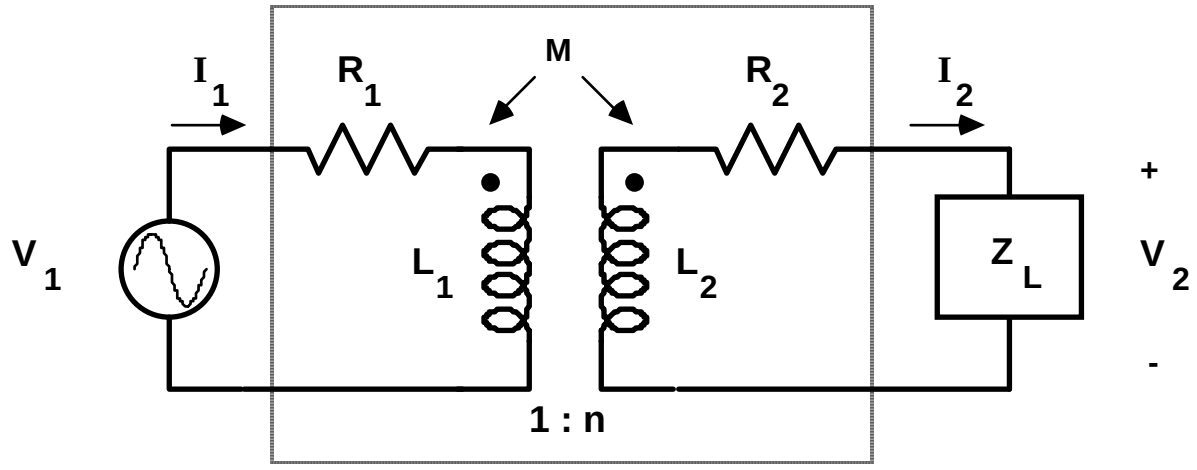


Figure 11.4

R_1, R_2, L_1 and L_2 model the resistive losses and inductance in the primary and secondary windings, respectively. The quantity M is the *mutual inductance* between the primary and secondary windings. The mutual inductance is given by

$$M = k \cdot \sqrt{L_1 L_2}\ ,$$

where k is the *coupling coefficient* of the particular transformer ($0 \leq k \leq 1$).

The basic equations for the transformer network of Figure 11.4 can be written using Kirchhoff's voltage law:

$$\mathbf{V_1} = (R_1 + j\omega L_1) \cdot \mathbf{I_1} - j\omega M \cdot \mathbf{I_2}$$

$$\mathbf{V_2} = j\omega M \cdot \mathbf{I_1} - (R_2 + j\omega L_2) \cdot \mathbf{I_2} = \mathbf{Z_L} \cdot \mathbf{I_2}$$

The negative sign on the $\mathbf{I_2}$ terms is due to our arbitrary definition of the secondary current as flowing out of the dotted terminal, while the primary current is defined to flow in. The parameters of this simple model can be measured as described below.

- The resistance terms R_1 and R_2 can be measured using an ohmmeter (DC) on the primary and secondary, respectively.

- If a voltage source is applied to the primary *while the secondary is left open-circuited ($\mathbf{I_2} = 0$)* the transformer equations reduce to:

  $$\mathbf{V_{1\,(oc)}} = (R_1 + j\omega L_1) \cdot \mathbf{I_1}$$

  $$\mathbf{V_{2\,(oc)}} = j\omega M \cdot \mathbf{I_1}$$

  If R_1 has been measured and we know the frequency ω, then measurements of $\mathbf{V_{1\,(oc)}}$, $\mathbf{V_{2\,(oc)}}$, and $\mathbf{I_1}$ can be used to determine the value of L_1 and M.

- If a voltage source is now applied to the secondary *while the primary is left open-circuited ($\mathbf{I_1} = 0$)* the value of L_2 can be determined in a similar fashion.

A Simple Line-Powered DC Supply

One common application of transformers is in power supply circuits. Many applications require either an AC or DC voltage source that must be derived from the available (in the USA) 110V rms 60 Hz sinusoidal voltage provided by the power company.

In addition to stepping up or down voltages, transformers also provide *electrical isolation* between the primary and secondary. Electrical isolation means that neither side of the secondary is connected to the primary power source. This is a very important safety consideration when powering electrical equipment from dangerously high voltages. In particular, isolation allows the secondary to receive its ground reference separately from the power source, thereby avoiding stray currents or unsafe power connections. The use of a third prong via the power plug is the recommended approach to provide safe grounding for the secondary.

As mentioned in Lab #5, a DC power supply can be created by peak rectifying an AC waveform. A simple low-voltage DC supply design utilizing a step-down transformer and a full-wave rectifier is shown in Figure 11.5.

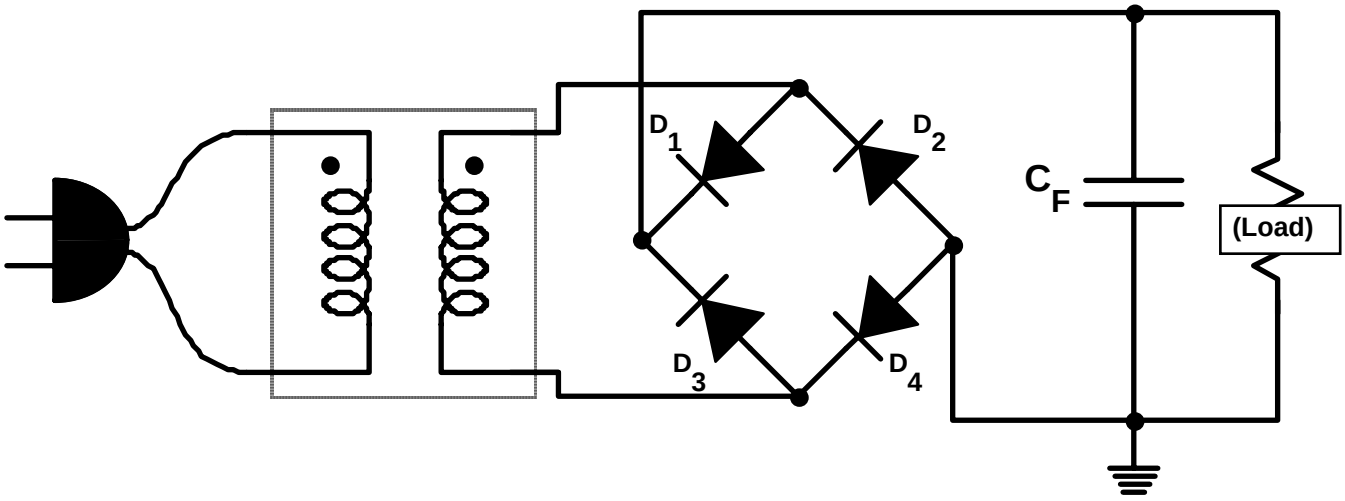


Figure 11.5

One problem with the supply of Figure 11.5 is that the output voltage across the load is not a pure DC value, but contains *ripple* due to the alternating charge-discharge cycles from the bridge rectifier. Furthermore, the circuit does not include any mechanism to maintain a constant output voltage as the load current varies or as the input line voltage fluctuates. To help solve these problems, a *voltage regulator* circuit is typically included between the filter capacitor, C_F, and the load in order to regulate the output voltage. Various types of voltage regulator circuits are available, including single integrated circuit devices.

REFERENCES

See Chapter 13 of the text by J. David Irwin, *Basic Engineering Circuit Analysis*, 4th ed., Macmillan Publishing Co., 1993 (pp. 581-623).

EQUIPMENT

Lab component kit (resistors, capacitor, diodes) Oscilloscope
Small power transformer Digital Multimeter (DMM) Function generator

PRE-LAB PREPARATION

(I) A step down transformer has a 120V rms primary voltage applied and a 12V rms voltage is measured at the secondary. Assuming the transformer can be considered ideal, determine the turns ratio, n.

If a 1Ω load is attached to the secondary of this transformer what is the rms load current? What is the rms primary current?

(II) The windings of a particular transformer are made from 30-gauge copper wire. The primary resistance is found to be 10Ω and the secondary resistance is 4Ω. Estimate the length of wire in the primary and secondary,* and estimate the number of turns in each coil assuming each turn requires on average 5 cm of wire. Also calculate the turns ratio.

(III) The DC resistance of the primary windings of a certain transformer is found to be 22Ω, while the resistance of the secondary windings is 0.8Ω. When a 60 Hz sinusoidal source is connected to the primary *with the secondary open circuited* and the primary voltage is adjusted to be 15V peak-to-peak, the primary current *entering at the dot* is found to be 35mA peak-to-peak, lagging the voltage by 87°. The open circuit voltage on the secondary is measured with a high-impedance 'scope probe to be 1.5 volts peak-to-peak. Then, by driving the secondary with the primary open circuited and the secondary voltage adjusted to be 2V peak-to-peak, the secondary current *entering at the dot* is found to be 20mA peak-to-peak, lagging the voltage by nearly 90°. From these measurements determine an estimate for the self-inductances (L_1 and L_2), the mutual inductance (M), and the coupling coefficient (k) of the transformer.

* 30-gauge wire is 0.25 mm in diameter. Copper has a resistivity of 1.7×10^{-6} Ω·cm. Can you figure out the resistance per unit length of the wire?

EXPERIMENT

The small power transformer used in this experiment is designed for 110V rms on the primary, producing about 12.5V rms on the secondary. The primary connections are the *black* wires and the secondary connections are the *red* wires. The secondary of this transformer is also equipped with a *center tap* connection. The center tap (*white*) is connected to the secondary windings halfway between each end, providing the possibility of obtaining ±6 volts with respect to the tap. Center tapped transformers are useful in the design of bipolar power supplies. In this experiment we will *not* be using the center tap: all secondary measurements should be made across the entire secondary (red to red).

(1) Determine the primary and secondary winding resistances R_1 and R_2 by using the multimeter to measure the DC resistance of the primary and secondary.

(2) Assemble the circuit of Figure 11.6. Adjust the function generator for a 60 Hz sinusoid with amplitude sufficient to produce a 2V peak-to-peak signal across the 100Ω series resistor. Measure the voltage across the primary [A-B] and the voltage across the secondary [C-D] in order to determine the turns ratio, *n*.

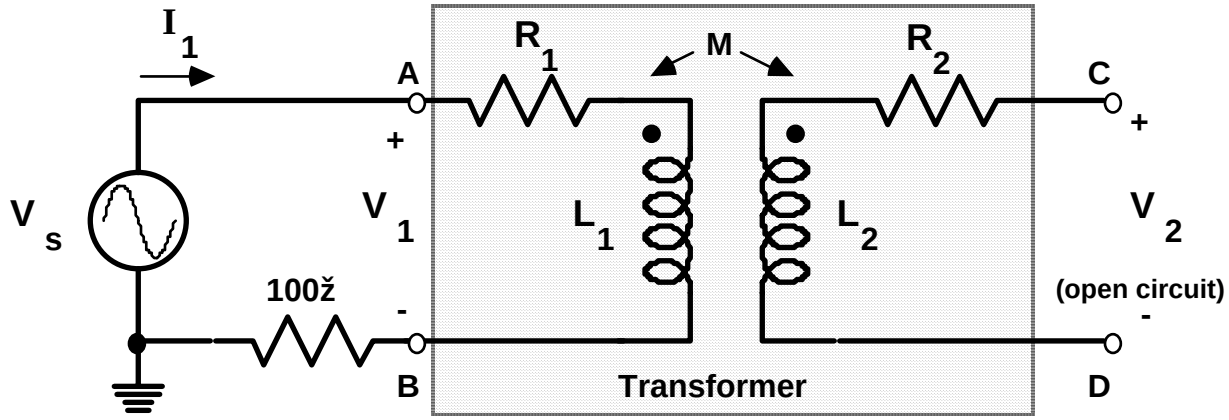


Figure 11.6

Use the phase measurement technique of Lab #10 to determine the input impedance of the transformer with the secondary open-circuited, i.e., trigger from A, then [A-B] = primary voltage, B/100Ω = primary current, and the phase difference between [A-B] and B is the phase difference between the primary voltage and current. Also re-measure the open-circuit secondary voltage [C-D]. From these measurements determine an estimate for the primary self-inductance, L_1, and the mutual inductance, M.

Next, reconnect the circuit to drive the secondary, leaving the primary open-circuited, as shown in Figure 11.7. Keep in mind the defined direction of $\mathbf{I_2}$. Make measurements to estimate the value of L_2 and M.

(3) Carefully measure the rms voltage of a standard 110V outlet. Plug the primary of the transformer into the outlet and measure the secondary rms voltage. Verify that the secondary voltage is approximately 12.5 volts rms. Now measure the secondary voltage for a range of resistors from your lab kit (be sure not to exceed the power dissipation limitation of the resistors!).

(4) Assemble the simple DC power supply circuit from the pre-lab, using several 22μF capacitors in parallel for the filter capacitor, C_F. Be sure to observe the correct polarity for the capacitors!!. Measure and sketch the ripple of the output waveform for a range of load resistances greater than 1kΩ, keeping in mind any effects due to the 1MΩ input resistance of the 'scope.

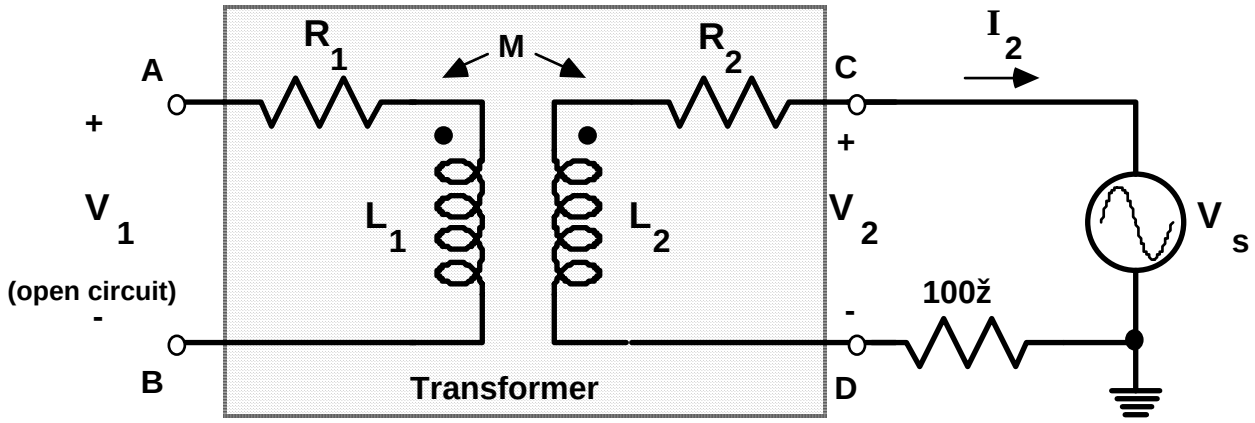


Figure 11.7

RESULTS

(a) Present your measurements and calculations of the transformer parameters. Explain your findings. Do your measurements of L_1, L_2, and M seem reasonable? What is your estimate of the value of the coupling coefficient, *k*? Are the results consistent with your expectations? Comment on the accuracy of the measurement procedure.

(b) Describe your measurements of the secondary voltage as a function of the load resistance from part 3. Does the transformer behave like an ideal voltage source here?

(c) Summarize your findings for the simple DC power supply you assembled in part 4. Explain your ripple measurements, and compare the results to the ripple concepts discussed in Lab #5.

(d) Suggest a few ways that this experiment can be improved.

Revised 7/94

Lab # 12
TITLE: Two-Port Parameters

ABSTRACT

Two-port description of an electrical network is a useful analytical tool in electrical engineering. This experiment considers the measurement issues related to two-port network descriptions, the relationship between the various two-port parameter definitions, and the use of equivalent two-port circuit models.

INTRODUCTION AND THEORY

A pair of terminals from a linear electrical network is referred to as a *port*. The voltage between the two terminals is the port voltage, and the current into the network is known as the port current. We require that Kirchhoff's current law be applicable at such a port, so whatever current enters the network on one of the port's terminals must exit the network on the other terminal. The conventional voltage and current definitions are indicated in Figure 12.1.

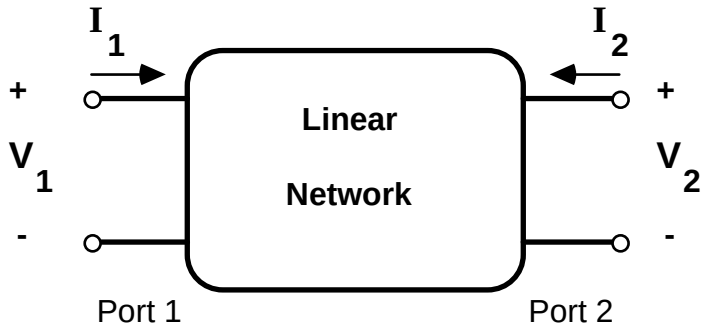


Figure 12.1

Note in particular that the direction of positive current is *into* the positive terminal of the port.

In general, a linear network can have an arbitrary number of ports. Since many problems in electrical engineering involve circuits which take an *input* signal and generate an *output* signal, we are typically most interested in *two-port* networks where one of the ports carries the input signal and the other port carries the output signal. In particular, the problem is to describe the mathematical relationships among the two port currents and the two port voltages.

It should be noted that the true significance of two-port network descriptions is found in the study of *circuit theory*: the generalization of all the circuit analysis tools you have been studying (KVL, KCL, Thèvenin, etc.) into a unified framework applicable to any circuit problem. In this way it is possible to tackle extremely complicated electrical networks in a proven, reliable, and consistent manner, rather than starting each problem from scratch. Moreover, the procedures for combining two-port networks with other networks can be expressed in terms of mathematical operations which are straight-forward to implement in computer software. For example, the SPICE circuit simulator internally represents the various circuit elements in terms of two-port matrices. The particular circuit topology you specify in the SPICE input file controls how the matrices are transformed and computed, but the actual computation procedure is applicable to any properly connected circuit configuration.

Two-Port Parameters: the Basic Configurations

The voltage and current relationships for two-port networks can be expressed in five basic forms:

(1) I_1 and I_2 due to V_1 and V_2 (admittance form)
(2) V_1 and V_2 due to I_1 and I_2 (impedance form)
(3) V_1 and I_2 due to I_1 and V_2 (hybrid form)
(4) I_1 and V_2 due to V_1 and I_2 (inverse-hybrid form)
(5) V_1 and I_1 due to V_2 and I_2 (transmission form)

Our choice among the four forms to represent a given network is arbitrary because we can easily convert from one form to another.

The mathematical representations corresponding to the five two-port forms are given below. The subscripted parameters in the equations (y_{xy}, z_{xy}, etc.) are called the *two-port parameters* for the particular form of representation.

Admittance:

$$\begin{cases} I_1 = y_{11}V_1 + y_{12}V_2 \\ I_2 = y_{21}V_1 + y_{22}V_2 \end{cases} \quad \text{or} \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

Impedance:

$$\begin{cases} V_1 = z_{11}I_1 + z_{12}I_2 \\ V_2 = z_{21}I_1 + z_{22}I_2 \end{cases} \quad \text{or} \quad \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Hybrid:

$$\begin{cases} V_1 = h_{11}I_1 + h_{12}V_2 \\ I_2 = h_{21}I_1 + h_{22}V_2 \end{cases} \quad \text{or} \quad \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Inverse-hybrid:

$$\begin{cases} I_1 = g_{11}V_1 + g_{12}I_2 \\ V_2 = g_{21}V_1 + g_{22}I_2 \end{cases} \quad \text{or} \quad \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

Transmission:

$$\begin{cases} V_1 = AV_2 - BI_2 \\ I_1 = CV_2 - DI_2 \end{cases} \quad \text{or} \quad \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

It is important to remember that because the elements in the linear two-port network are frequency-dependent in general (e.g., capacitors and inductors), the two-port parameters are also frequency-dependent. Thus, measurements of the two-port parameters will need to cover the desired range of response frequencies.

The parameters for a two-port network can be determined by applying pairs of excitation signals and measuring pairs of response signals. For example, if we wanted to determine the *impedance* parameter z_{11} for a two-port network we can solve the first port equation for z_{11} to yield

$$V_1 = z_{11}I_1 + z_{12}I_2$$
$$\Rightarrow \quad z_{11} = \frac{V_1 - z_{12}I_2}{I_1} \quad .$$

If we let $I_2 = 0$, which means that we let port 2 be an open circuit (no current) during the measurement, then z_{11} is the complex ratio of V_1 and I_1. The z parameter measurements can be summarized:

- z_{11}: Set $I_2 = 0$ (open circuit), apply V_1 or I_1, and measure ratio $\left(z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} \right)$

- z_{12}: Set $I_1 = 0$, apply V_2 or I_2, and measure ratio $\left(z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} \right)$
- z_{21}: Set $I_2 = 0$, apply V_1 or I_1, and measure ratio $\left(z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} \right)$
- z_{22}: Set $I_1 = 0$, apply V_2 or I_2, and measure ratio $\left(z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0} \right)$

Of course, a similar procedure can be developed for the other forms of two-port networks.

The Hybrid Parameters and Small-Signal Transistor Models

The hybrid two-port parameters involve exciting the network with the current I_1 and the voltage V_2, resulting in the voltage V_1 and the current I_2. This representation is similar to the active-mode behavior of bipolar junction transistor small-signal amplifiers, so AC hybrid parameters are often used to describe BJT operating characteristics. The small-signal simplified hybrid-π model of the BJT was considered in Lab #6. The simple model is repeated here in Figure 12.2, including the non-infinite output resistance, r_o.

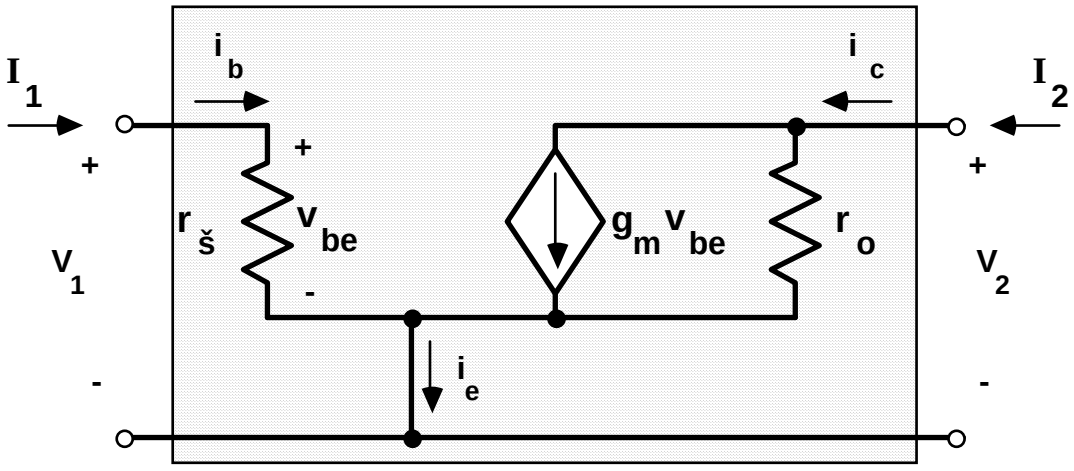


Figure 12.2

Note that the two ports share a common node at the emitter. Also, it is apparent that the port current I_1 is i_b and current I_2 is i_c in the BJT AC small-signal model. It is also clear that the port voltages V_1 and V_2 are v_{be} and v_{ce} in the model, respectively. Rewriting the hybrid equations,

$$\begin{cases} V_1 = h_{11} I_1 + h_{12} V_2 \\ I_2 = h_{21} I_1 + h_{22} V_2 \end{cases} \quad \text{becomes} \quad \begin{cases} v_{be} = h_{11} i_b + h_{12} v_{ce} \\ i_c = h_{21} i_b + h_{22} v_{ce} \end{cases}.$$

Then, since we already know that for the BJT AC small-signal model $v_{be} = r_\pi \cdot i_b$ and $i_c = \beta \cdot i_b + v_{ce}/r_o$, the hybrid two-port parameters of the simple model in Figure 12.2 are given by

$$h_{11} = r_\pi, \qquad h_{12} = 0,$$
$$h_{21} = \beta, \quad \text{and} \quad h_{22} = 1/r_o.$$

The importance of this result is that if we can measure the hybrid two-port parameters of a biased BJT amplifier, then we can use the results to estimate the small-signal quantities of the transistor model.

It should also be noted that at high frequencies (f > 50kHz or so) the internal capacitance of the semiconductor junctions and packaging can become a significant factor in the small-signal model. At "low" frequencies (f < 10kHz) we will neglect the effects of capacitance and concentrate on the resistive elements of the model. A more complete AC small-signal model appropriate for the relatively low frequency range is shown in Figure 12.3. Note the inclusion of a resistance, r_{bb}, in series with the base and a base-collector resistor, r_μ. Resistor r_{bb} is used to model the nonzero resistance of the base material and electrical contacts, while r_μ models the effect of the collector voltage on the base. Since r_{bb} is typically much smaller than r_π, and r_μ is typically much greater than r_o, it is often OK to neglect these elements—as we have until now.

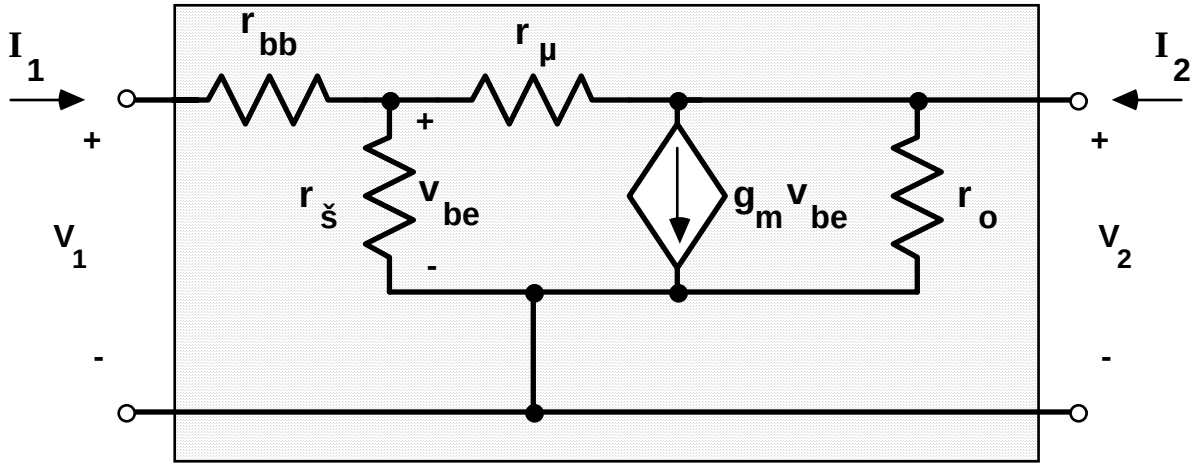


Figure 12.3

Manufacturers of transistors typically use the hybrid parameters on the data sheet to report the performance of BJTs. Instead of using the numerical subscripts, however, the conventional method is to express the hybrid equations as

$$\begin{cases} v_{be} = h_{ie} i_b + h_{re} v_{ce} \\ i_c = h_{fe} i_b + h_{oe} v_{ce} \end{cases},$$

where the subscript *i* indicates *input*, *o* indicates *output*, *f* indicates *forward*, *r* indicates *reverse*, and the common subscript *e* denotes the *common-emitter* port arrangement.* The data sheet generally indicates the conditions under which the parameters were determined, such as DC collector current and temperature.

If we include r_{bb} and r_μ in the hybrid parameter derivation we find the following relationships.

$$h_{ie} = h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0}$$

h_{ie}: From the definition , we see that we need to find the input impedance at port 1 with a short-circuit ($V_2 = 0$) applied at port 2. The result is that $\mathbf{h_{ie} = r_{bb} + (r_\pi \| r_\mu)}$. Note that if we assume $r_\pi << r_\mu$ and $r_\pi >> r_{bb}$, then $h_{ie} \approx r_\pi$ as was found for the simple equivalent circuit.

* Note that the AC hybrid parameters use small-letter subscripts. Some manufacturers also report DC quantities using capital subscripts (such as forward current gain, h_{FE}).

$$h_{re} = h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

h_{re}: This parameter is defined , which means that we need to find the voltage V_1 due to V_2 with port 1 open circuited ($I_1 = 0$). This is simply the voltage divider of r_π and r_μ since no current flows in r_{bb}: **$h_{re} = r_\pi/(r_\pi+r_\mu)$**. Again, if we assume that $r_\pi << r_\mu$ then $h_{re} \varnothing 0$ as we found before.

$$h_{fe} = h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$$

h_{fe}: The short-circuit current gain is defined . Writing node equations for I_2 and I_1:

$$I_2 = g_m v_{be} - v_{be}/r_\pi$$
$$I_1 = v_{be}/(r_\pi \| r_\mu)$$

resulting in

$$h_{fe} = \frac{g_m - 1/r_\pi}{1/\left(r_\pi \| r_\mu\right)} = \frac{g_m r_\mu r_\pi - r_\pi}{r_\mu + r_\pi} = \frac{\beta r_\mu - r_\pi}{r_\mu + r_\pi}.$$

Note that $h_{fe} \approx \beta$ if we again assume that $r_\pi << r_\mu$.

$$h_{oe} = h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

h_{oe}: Finally, using the definition and equation for I_2 in terms of V_2 (with port 1 open circuited):

$$I_2 = V_2 \cdot [\, 1/r_o + 1/(r_\pi+r_\mu) + g_m r_\pi/(r_\pi+r_\mu) \,],$$

we have **$h_{oe} = [\, 1/r_o + 1/(r_\pi+r_\mu) + \beta/(r_\pi+r_\mu) \,]$**, or **$h_{oe} \approx 1/r_o + \beta/(r_\pi+r_\mu)$** if $\beta >> 1$. As before, if r_μ is assumed to be much greater than r_π then $h_{oe} \approx 1/r_o + \beta/r_\mu \approx 1/r_o$.

Collecting all the relationships we can solve for the BJT small-signal model parameters using the measured DC bias collector current, I_C, and the measured h-parameters:

$$g_m = \frac{I_C}{V_T} \qquad (V_T \approx 25\text{mV})$$

$$r_\pi = \frac{h_{fe}}{g_m} \qquad r_\mu = \frac{r_\pi}{h_{re}}$$

$$r_o = \frac{1}{\left(h_{oe} - \frac{h_{fe}}{r_\mu} \right)} = \frac{V_A}{I_C} \qquad r_{bb} = h_{ie} - r_\pi$$

Note that r_o is most easily determined from V_A/I_C.

Measurement Issues for BJT Two-Port Parameters

In order to actually measure the hybrid parameters for a biased BJT it is important to avoid changing the DC bias conditions during the measurement. For example, to determine h_{ie} from the equation $v_{be} = h_{ie}\, i_b + h_{re}\, v_{ce}$ we may be tempted to simply force v_{ce} to be zero by shorting the collector to the emitter, then measure $h_{ie} = v_{be}/i_b$. However, shorting the collector to the emitter saturates the transistor and destroys the DC bias conditions. Instead, we must use an "AC short circuit", e.g., a capacitor, from collector to emitter so that the DC bias conditions are maintained, while the AC model "sees" zero volts across port 2.

REFERENCES

See Chapter 7 (§ 7.5) of the text by Sedra and Smith, *Microelectronic Circuits*, 3rd ed., Saunders College Publishing (Holt, Rinehart, and Winston), 1990.

See also Chapter 15 of the text by J. David Irwin, *Basic Engineering Circuit Analysis*, 4th ed., Macmillan Publishing Co., 1993 (pp. 729-769).

EQUIPMENT

Lab component kit	Multimeter	Power supply
Function generator	Oscilloscope	Heathkit trainer
LC meter	Curve tracer	

PRE-LAB PREPARATION

(I) Determine the *impedance* (*z*) and *hybrid* (*h*) two-port parameters for the network in Figure 12.4.

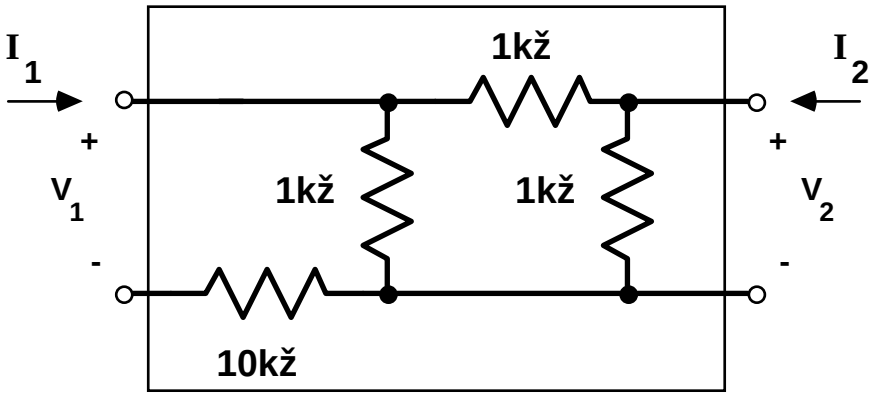


Figure 12.4

(II) Next, determine the *impedance* (*z*) and *hybrid* (*h*) two-port parameters for Figure 12.5.

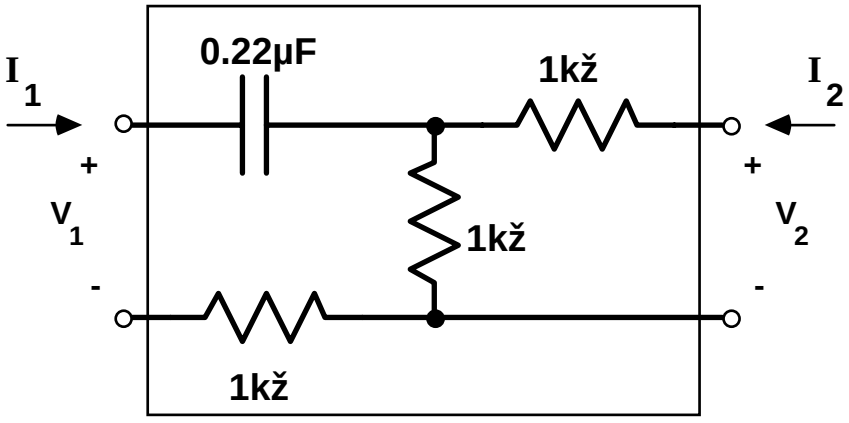


Figure 12.5

(III) In order to measure the small-signal h-parameters for a biased BJT we will use the two circuits of Figure 12.6a and b.

- Choose resistors R_B and R_C from the 5% tolerance resistors (or combinations) in your kit so that the DC bias conditions are $I_C \approx 10mA$ and $V_C \approx 9$ volts, assuming $V_{BE} = 0.7$ volts, $V_{CC} = 18$ volts, and $\beta = 100$.

- For the measurements on Figure 12.6a, we want $R_S << R_B$ and $R_L << R_C$ so that the AC small-signal current in R_S is essentially i_b and the small-signal current in R_L is essentially i_c. Thus, choose R_L to be about $R_C/10$, and R_S to be about $R_B/10$. Use 22μF capacitors for C_B and C_C.

  Now show how you can determine expressions for the AC small-signal BJT parameters h_{fe} and h_{ie} from measurements of v_x, v_b, and v_o in the circuit of Figure 12.6a.

- The circuit of Figure 12.6b can be used to determine the AC small-signal BJT parameter h_{re}, assuming that R_B and the oscilloscope impedance are both >> r_π so that the base "sees" an open circuit (port 1 current must be zero for h_{re}). Find the simple expression for h_{re} in terms of AC voltages from the Figure.

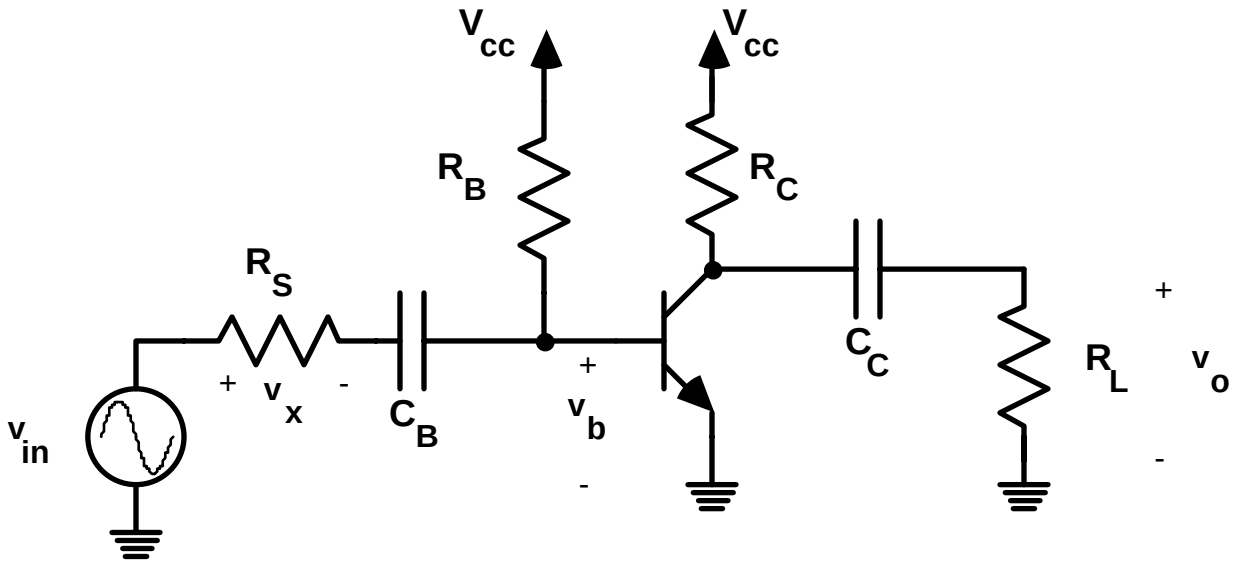


Figure 12.6a

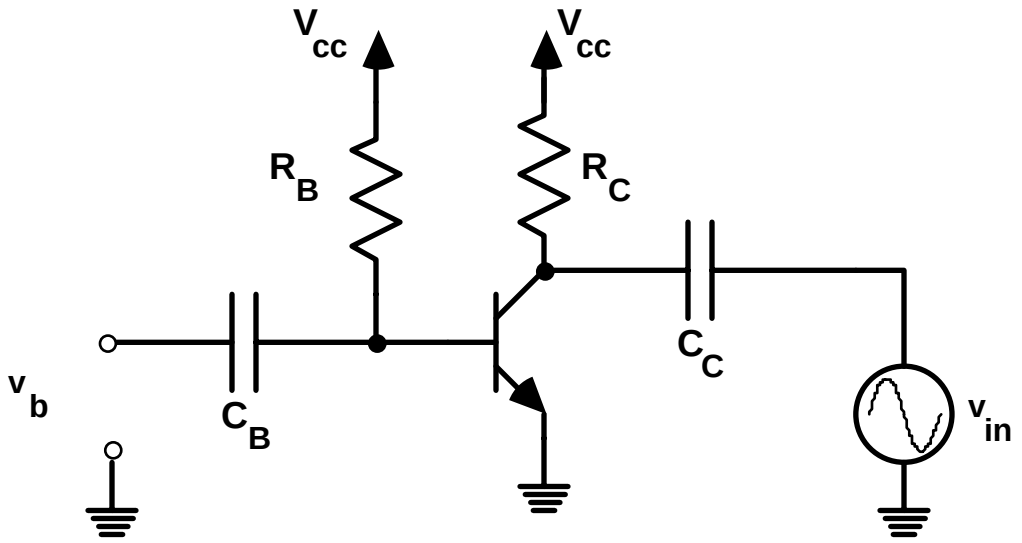


Figure 12.6b

(IV) Sketch the AC small-signal models of Figures 12.6a and b. Label the components, nodes, currents, and voltages.

EXPERIMENT

(1) Assemble the circuit of Figure 12.4 and perform measurements to find the DC impedance parameters (*z*) of the network. Record the actual values of the components used.

(2) Assemble the circuit of Figure 12.5 and perform measurements of the AC (magnitude only) hybrid parameters (*h*) of the network at 1kHz, 2kHz and 5kHz. You will need to measure both AC voltages and currents, so think about how best to approach the measurements. Record the actual values of the components used.

(3) Use the curve tracer instrument in the lab to obtain a plot of I_C vs. V_{CE} for your BJT. From the measurement estimate the value of β and V_A.

(4) Using the measured value of β, choose the four resistors for the circuit of Figure 12.6a using the guidelines as you did in the pre-lab. Assemble the circuit and adjust R_C and R_B as necessary to obtain $I_C \approx 10$ mA and $V_C \approx 9$ volts. Adjust the function generator for an AC small signal input to the circuit at 10kHz. Use the scope (AC coupling) or the DMM (AC) to measure v_x, v_b, and v_o in order to estimate h_{fe} and h_{ie} using the expressions you determined in the pre-lab.

(5) Now keep the same values of R_B and R_C and reconnect your circuit according to Figure 12.6b. Carefully measure the required quantities to estimate h_{re}.

RESULTS

(a) Discuss your measured impedance parameters for part 1. How do your measurements compare to your expectations?

(b) Present your AC hybrid parameter measurements from part 2. Describe how you measured the magnitude of the signals. If the circuit was actually an unknown network sealed in a box and you only had access to the two ports, would you need to change your measurement technique? What if the *phase* of the hybrid parameters was to be measured?

(c) Explain your measurements of parts 3 - 5 and present your estimates of the small-signal model parameters r_{bb}, r_π, g_m, r_μ, and r_o. Do your model parameters make sense? What types of errors might be involved in your measurements, e.g., can r_{bb} and r_μ be determined accurately?

(d) What are the aspects of this experiment that should be improved?

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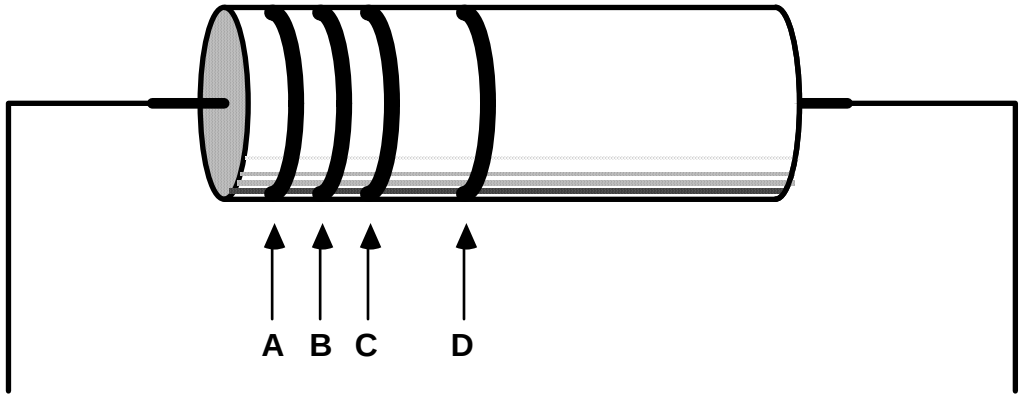
Appendix
TITLE: Resistor Color Bands

Resistors are labeled with an approximate, or *nominal*, resistance value and a *tolerance* specification. For example, a resistor might be labeled as 1kΩ +/- 5%, meaning that the manufacturer guarantees that the actual resistance will be between 950Ω (1kΩ - 5%) and 1,050Ω (1kΩ + 5%). The nominal resistance value and its tolerance for 5, 10, and 20% resistors are either printed numerically on the resistor body (if the resistor is large enough), or indicated by four colored bands (ABCD) on the resistor body.



Resistance = $AB \times 10^{C} \pm$ tolerance (D)

The numerical values corresponding to the colors are:

0 ∅	Black	5 ∅	Green	Tolerance:	
1 ∅	Brown	6 ∅	Blue	20% ∅	No band
2 ∅	Red	7 ∅	Violet	10% ∅	Silver
3 ∅	Orange	8 ∅	Gray	5% ∅	Gold
4 ∅	Yellow	9 ∅	White		
		-1∅	Gold		

For example, a 1kΩ ± 5% resistor [10×10^{2}] is labeled BROWN:BLACK:RED:GOLD, a 220Ω ± 10 % resistor is labeled RED:RED:BROWN:SILVER, and a 1Ω ± 5% resistor must be represented as [10×10^{-1}], or BROWN:BLACK:GOLD:GOLD.

Resistors are also available in 1% tolerance values. The 1% resistors have five colored bands (JKLMN) instead of four and indicate the resistance value as JKL x 10^{M} Ω, with the tolerance band (N) colored BROWN.

If we test many resistors with the same nominal (labeled) value we will find that the *actual* resistance varies from resistor to resistor within the tolerance range. On the other hand, the resistance value of a *particular* resistor is usually quite constant with time, staying close to its original measured value.

Resistors are also rated according to their maximum power dissipation. Most of the resistors used in this course are 0.25 watt devices, meaning that they can safely handle up to one-quarter watt of power. Resistors with lower and much higher power ratings are available, with the resistor size increasing with the power rating.

It is important to realize that only a limited number of nominal resistances are available. Manufacturers produce *standard* values that are spaced by approximately twice the tolerance specification (a logarithmic spacing) so that a wide range of resistances are covered by a minimum number of nominal values. The standard 5% resistors, for instance, follow the pattern:

1.0	1.6	2.7	4.3	6.8
1.1	1.8	3.0	4.7	7.5
1.2	2.0	3.3	5.1	8.2
1.3	2.2	3.6	5.6	9.1
1.5	2.4	3.9	6.2	10.0

which then repeats for each greater power of 10.

Appendix II
TITLE: A Few Pointers for Using PSpice

ABSTRACT

PSpice is a useful program for analyzing electronic circuits. A good working knowledge of the capabilities of PSpice can be very helpful in the process of designing and debugging circuits and subsystems. The basics of operating PSpice have been covered in previous courses, so refer to your course notes and textbooks for introductory information. This appendix includes a few suggestions and pointers that are intended to help you obtain useful results quickly and reliably. Of course, entire books are written on PSpice: this appendix can only scratch the surface.

INTRODUCTION AND THEORY

SPICE is an acronym for ***S****imulation* ***P****rogram - **I**ntegrated **C**ircuit **E**mphasis*. It was developed at the University of California - Berkeley as a way to test and evaluate designs for integrated circuits before actually fabricating the ICs: it is far cheaper to discover and correct problems using software simulation than to fabricate and test each new design. Versions of SPICE are available for almost every type of computer, from small PCs to workstations to supercomputers. Although many other circuit simulators are now available, SPICE was the first to gain widespread acceptance and to become an industry standard.

SPICE is based on a set of software *models* for various circuit elements. Built-in models include independent and dependent voltage and current sources, resistors, inductors, capacitors, transformers, and semiconductors (diodes, transistors, etc.). All of the models are described by various user-specified parameters. For example, the resistor model is essentially Ohm's law, where the user specifies the resistance value. Like most SPICE models, the resistor model contains more sophisticated features, like a temperature coefficient to indicate the change of resistance as a function of temperature. In general the SPICE models contain reasonable *default* values so that the user need only specify the parameters of interest.

SPICE is able to perform several different types of simulation: DC, AC small signal, transient, sensitivity, noise, distortion, etc. Several example simulations are presented later.

SPICE on microcomputers: PSpice

The version of SPICE available on the department's microcomputers, PSpice, has several features that may be different from the original SPICE versions which were designed to run on mainframe computers. In particular, the PROBE feature is a useful way to obtain plots and graphs of the simulation results. The version of PSpice available on the PCs is an evaluation system suitable for relatively simple circuits. Several limitations on the number of circuit nodes and components are present in the evaluation version that are not present in the actual commercial version of the software. This student version is not protected by the manufacturer and you are welcome to make a free copy for yourself if you have your own PC at home.

PSpice on the PCs includes a *library* of several "subcircuits". The subcircuits are accurate models of complicated components such as op amps. One of the available models is the **uA741**, which is a model of an actual 741 op amp. To use the library include a line in your input file:

```
.LIB EVAL.LIB
```

This causes PSpice to load in the subcircuit definitions from the file eval.lib. The library eval.lib is simply a text file containing SPICE subcircuit definitions, so you can look at the file with any text editor.

To use the 741 subcircuit, for example, you need to make the following connections:

```
XOPAMP n1 n2 n3 n4 n5 uA741
```

where *n1* = noninverting input
n2 = inverting input
n3 = positive power supply
n4 = negative power supply
n5 = output
are the node numbers from your circuit.

The specific subcircuit name "XOPAMP" is not important, but you must use a name beginning with "X", which is the SPICE convention for subcircuit calls. The uA741 name tells SPICE that you will be using the 741 model from the EVAL.LIB file.

Types of SPICE Elements

PSpice recognizes many types of electrical elements based on the first letter used for the element name. The list of first letters is given below.

Letter	Element type
B	GaAs FET (Gallium Arsenide Field-Effect Transistor)
C	Capacitor
D	Diode
E	VCVS (Voltage-controlled voltage source)
F	CCCS (Current-controlled current source)
G	VCCS (Voltage-controlled current source)
H	CCVS (Current-controlled voltage source)
I	Independent current source
J	JFET (Junction Field-Effect Transistor)
K	Coupling coefficient for mutual inductance
L	Inductor
M	MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor)
Q	BJT (Bipolar Junction Transistor)
R	Resistor
S	Voltage-controlled switch
T	Transmission line
V	Independent voltage source
W	Current-controlled switch

You should refer to a PSpice book or manual to find out the correct parameters associated with each type of element.

Types of PSpice Analysis

AC, DC, TRAN, etc.
distortion, fourier

Useful Features of PROBE

REFERENCES

probe: mathematical operations on signals

It is vital to realize that a circuit simulator such as SPICE is only a tool: **YOU** must specify the circuit interconnections, choose the parameters, and evaluate the results. This means that you must know what to expect in the SPICE output, and what circuit parameters to change if the results are not acceptable. Sitting at a terminal and randomly changing parameters in hope of coming up with good results is *not* the strategy of an electrical *engineer*. In short, you must still provide the design, correctly specify the circuit for SPICE, and interpret the results. This means maintaining good documentation and program comments, performing a quick hand analysis to verify that the SPICE results are reasonable, and understanding the limitations of the SPICE models.

Diodes and SPICE

SPICE includes a built-in diode model. The model implements the basic junction diode equation, except SPICE uses the symbol **IS** for I_s, and **N** for n. A diode is declared in SPICE as:

```
Dname   +node  -node  modelname
...
.MODEL  modelname  D  (IS=xx, N=yy),
```

where *+node* and *-node* are the node numbers connected to the anode and cathode of the diode, respectively. The name of the diode (D*name*) is up to you, except that the first letter must be a D. You are also free to choose the name of the model.

The SPICE diode model also has numerous other parameters besides the basic diode equation. For example, the SPICE diode can simulate operation in the breakdown region, if desired.

BJTs and SPICE

SPICE includes an extensive BJT model. The model implements the basic bipolar junction transistor equations, with the symbol **IS** for I_s, **BF** for β, and **VAF** for the Early voltage, V_A. A BJT is declared in SPICE as:

```
Qname   NC NB NE  modelname
...
.MODEL  modelname  type  (IS=xx, BF=yy, VAF=zz)
```

where *NC*, *NB*, and *NE* are the node numbers connected to the collector, base and emitter, respectively. The name of the BJT (**Q***name*) is up to you, except that the first

letter must be a **Q**, and you are also free to choose *modelname*, the name of the model. The *type* is either **NPN** or **PNP**.

The SPICE BJT model has numerous other parameters that are used to describe the operation of BJTs in various configurations, frequency ranges, etc. The library of device models supplied with the student version of PSpice (EVAL.LIB) contains several more complete transistor models for actual transistors.

MOSFETs and SPICE

Several models applicable to FETs are available using SPICE. The built-in models implement the basic triode and saturation equations, including the more complicated behavior found in actual devices. The basic SPICE format for MOSFETs is:

```
Mname   ND NG NS NB  modelname
...
.MODEL  modelname  type  (VTO=xx, KP=yy)
```

where *ND*, *NG*, *NS*, and *NB* are the node numbers connected to the drain, gate, source and substrate (body), respectively. For our purposes, the source and body should be connected together, i.e., *NS* and *NB* should be the same. The name of the MOSFET (**M***name*) is up to you, except that the first letter must be **M**, and you are also free to choose *modelname*, the name of the model. The *type* is either **NMOS** or **PMOS**.

The model parameter **VTO** is the threshold voltage for the device (V_t). Recall that V_t is positive for enhancement *n*-channel devices and negative for depletion *n*-channel devices (and vice versa for *p*-channel devices). The parameter **KP** is *twice* the parameter K used in the triode and saturation equations (**KP** = 2K)* .

The SPICE MOSFET model has other parameters and features that are used to describe the operation of MOSFETs in various configurations, frequency ranges, etc.

* Actually, $K = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)$, while $\mathbf{KP} = \mu_n C_{ox}$. We are tacitly assuming that the width and length of the channel are the same for the simple SPICE model that is adequate for this experiment.