A Power-Efficient Design Approach to Radiation Hardened Digital Circuitry using Dynamically Selectable Triple Modulo Redundancy

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Abstract- Triple Modulo Redundancy (TMR) is one of the most common techniques for fault mitigation in digital systems. TMR-based computing has a natural application to mission critical systems for military and aerospace applications which are exposed to cosmic radiation and are susceptible to Single Event Upsets (SEUs). TMR's increased immunity to SEUs comes at the expense of increased power consumption and area. This paper presents a dynamically selectable TMR architecture which can be used to reduce power consumption when radiation levels are low. We apply this architecture to a test system in order to evaluate its power reduction and area overhead compared to a traditional static TMR approach. We show that the dynamically selectable TMR can be adopted with only a 2.2% increase in equivalent gate count compared to the traditional static TMR when implemented on a Xilinx Virtex-4 FPGA. This approach yields as much as a 67% reduction in power consumption versus a traditional static TMR approach when radiation levels are low.

I. INTRODUCTION

Recently, there has been an increased interest in the radiation immunity of digital circuitry for use in aerospace and military applications [1,2]. This renewed interest comes as a result of two main factors. The first is the widening gap between the performance of commercial off-the-shelf (COTS) integrated circuits and those that are fabricated with the ability to withstand the radiation levels of an extraterrestrial environment [3]. The second reason is that the number of foundries providing radiation hardened (RadHard) processes is diminishing due to a reduction in post cold war Department of Defense funding.

As scientists and engineers re-approach the problem of radiation immunity in digital circuits, there are a new set of constraints and opportunities that are present that must be addressed. First, creating an infrastructure of foundries that are capable of producing a Radiation Hardened processes is economically infeasible due to the low volume nature of the military/aerospace applications. Further, the security issues surrounding the military/aerospace applications prevent the outsourcing of fabrication to lower labor cost regions of the globe [1,2,3]. This economic constraint is mandating that approaches to radiation tolerance be developed that use domestic CMOS processing capability. This allows the solutions to scale with the advances being made in fabrication technology while still maintaining economic feasibility. While this presents a new constraint on solutions, it also opens up an opportunity to exploit the circuit density available in modern CMOS processes.

One logical approach that has been adopted as a formidable solution to radiation tolerance of Single Event Transients (SETs) and Single Event Upsets (SEUs) is *Triple Modulo Redundancy (TMR)* [4,5,6,7]. TMR is an approach where 3 identical circuits are used for each logic operation. The outputs of the 3 identical logic circuits are fed into a voting system which produces an output based on the majority of values. This technique assumes that a radiation particle will only strike the diffusion region of one of the circuits creating an SEU. Since the other two circuits in this approach are unaffected, the voting system will disregard the inconsistent result of the effected circuit and produce the correct output. This approach has been proven and implemented in modern FPGAs [8].

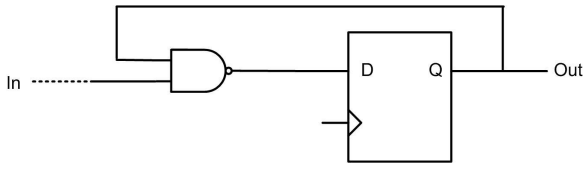

Figure 1. Example Circuit without Radiation Tolerance

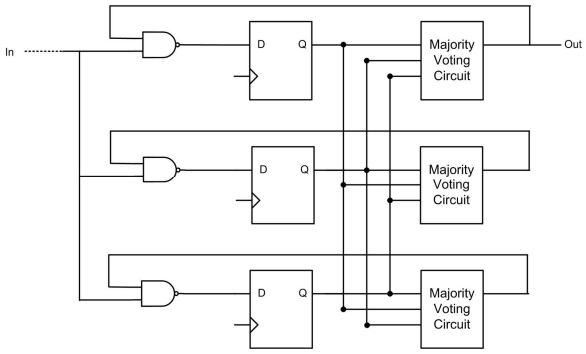

Figure 2. Example Circuit with Radiation Tolerance using Static Triple Modulo Redundancy (TMR)

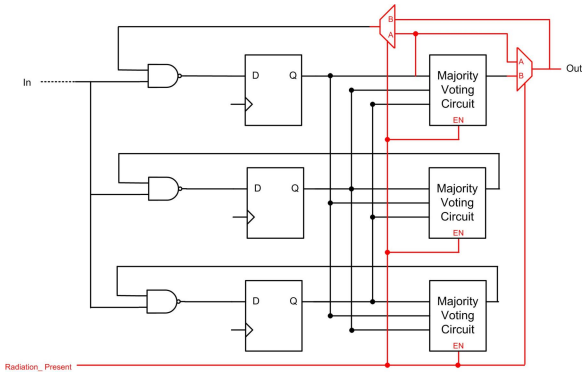

Figure 3. Example Circuit with Radiation Tolerance using Low Power, Dynamic Triple Modulo Redundancy

The drawback of this approach is the increased area and power consumption associated with having three redundant circuits and the additional voting hardware. While the increase in area is not necessarily a problem due to the high density of modern processes, the power consumption of extra circuitry is a detrimental issues to satellite and mission spacecraft running on portable power cells [1,2].

In this paper, we present novel solution to radiation tolerance based on the TMR approach in order to reduce overall power. In our approach, we propose a dynamically selectable TMR circuit that is under the control of a built in current sensor (BICS) [6] that detects when radiation is present. Under normal operation (i.e., no radiation detected), the TMR circuitry is disconnected from the main logic path, thus consuming no extra power from the system. When the BICS detects radiation, the TMR circuitry is enabled and redundancy checking is performed. This approach allows the average power of the system to be reduced by not using TMR checking when the circuit resides in a radiation free environment. This approach uses slightly more area than a straight TMR approach; however, the power consumption is reduced considerably. This type of logical solution is ideal for implementation in COTS FPGAs. Figure 3 shows the architecture of the dynamic TMR approach. We apply this approach to an 8-bit counter design to evaluate the implementation details, the area impact, and power consumption. We use VHDL to describe the system and implement the design on a Xilinx Virtex-4 FPGA in order to evaluate the area and power consumption of our approach.

II. DESIGN APPROACH

Our system is based on the existence of an external radiation sensor which can detect when radiation is present and will produce a control signal for the dynamic TMR system [6]. This signal is used by the dynamic TMR system to know when to switch between standard operation and TMR. The signal is assumed to be high for multiple system clock cycles so that it can be used as a synchronous control input.

Under normal operation (no radiation), the system only uses one of the three redundant circuits. The outputs of this active circuit (#1) are used as the final outputs of the system. The TMR voting machine is not used in this case. The other two redundant circuits (#2 & #3) are disabled. By disabling the two redundant circuits and the TMR voting machine, power consumption can be reduced when the system resides in a radiation free environment.

When the system resides in a heavy radiation environment, the system is switched into TMR mode by the sensor control signal. The system first enables the two redundant circuits and then loads them with the current information in circuit #1. This step initializes circuits #2 and #3 so that they can be used for redundancy checking. The final step is to activate the voting machine. Once the voting machine is enabled, the system operates as a traditional TMR system. During operation in a radiation environment, the voting machine has the capability to re-load any of the circuits with the majority result in the case that a radiation strikes causes corrupt information.

III. TEST SYSTEM

We applied our dynamic TMR approach to a standard 8-bit up/down counter with enable and load capability. This type of circuit is one of the main components for any stored program computer in order to handle Program Counter (PC) and Stack Counter (SP) operation. The counter was designed in VHDL. We inserted the ability to mimic a radiation strike within the counter by adding a random value to the counter by the test bench. The following VHDL code shows how the radiation was optionally inserted into the 8-bit counter design.

VHDL 1 8-Bit Counter with Radiation Error

```
process (clock, reset)
 begin
   if (reset = '0') then
      count_int <= x"00";
   elsif (clock'event and clock = '1') then
      if (en = '1')  then
         if (load = '1') then
             count_int <= count_in;
         elsif (inc_dec='1') then
             count_int <= count_int + 1 + rad;
         else
             count_int <= count_int - 1 + rad;
          end if;
      end if;
   end if;
end process;
```

A VHDL segment for the Voting and TMR control decision is given below. This subsystem handles the enabling and loading of the two redundant counters when the radiation control signal is asserted.

Algorithm 1 Voting and TMR Control

```
if ((in1 = in2) != in3) then   “cnt 3 is corrupted”
    disable counter #1 & #2
    enable counter #3
    load counter #3 with value in counter #1
    enable counter #1 & #2

elsif ((in1 = in3) != in2)     “cnt 2 is corrupted”
    disable counter #1 & #3
    enable counter #2
    load counter #2 with value in counter #1
    enable counter #1 & #3

elsif ((in2 = in3) != in1)     “cnt 1 is corrupted”
    disable counter #2 & #3
    enable counter #1
    load counter #1 with value in counter #2
    enable counter #2 & #3

end if
```

The system was simulated using the *Aldec ActiveHDL* software. The following logic simulation waveforms shows the operation of our system. Figure 4 shows the normal operation of the system when there is no radiation present. This mode represents the low-power mode. Figure 5 shows the steps that the system takes when the radiation detection signal is asserted. This control signal indicates that the TMR control circuitry must enable the two redundant counters, load them with the value from counter #1, and then begin producing a system output based on the majority vote of the three redundant counters. Figure 6 shows the operation of the system when it resides in a heavy radiation environment. In this mode of operation, the TMR system produces an output based on the majority vote of the three redundant circuits. When one of the counters produces an inconsistent result, the TMR control circuit attempts to reload the effected circuit. Figure 6 shows a radiation strike on counter #3 and how the TMR control circuit reloads the effected circuit.

IV. IMPLEMENTATION & RESULTS

We implemented our dynamic TMR system on a *Xilinx Virtex-4 FPGA*. We also implemented a traditional static TMR system on the same FPGA to compare the impact on area that the dynamic approach has. Table 1 lists the area usage that both approaches take when targeting a Virtex-4 FPGA. This table shows that the dynamic TMR only takes 2.2% more equivalent gates compared to the static TMR.

The dynamic TMR has the ability to disable two of the three redundant circuits in any system. By disabling these systems, no AC power is consumed. This architecture as the potential to reduce the power consumption by 66% through disabling redundancy in low radiation environments. The only incremental control circuitry that is required is the ability to disable and the redundant circuits and initialize these circuits when radiation is detected. This additional control logic is negligible compared to the size of the logic in the actual counters themselves.

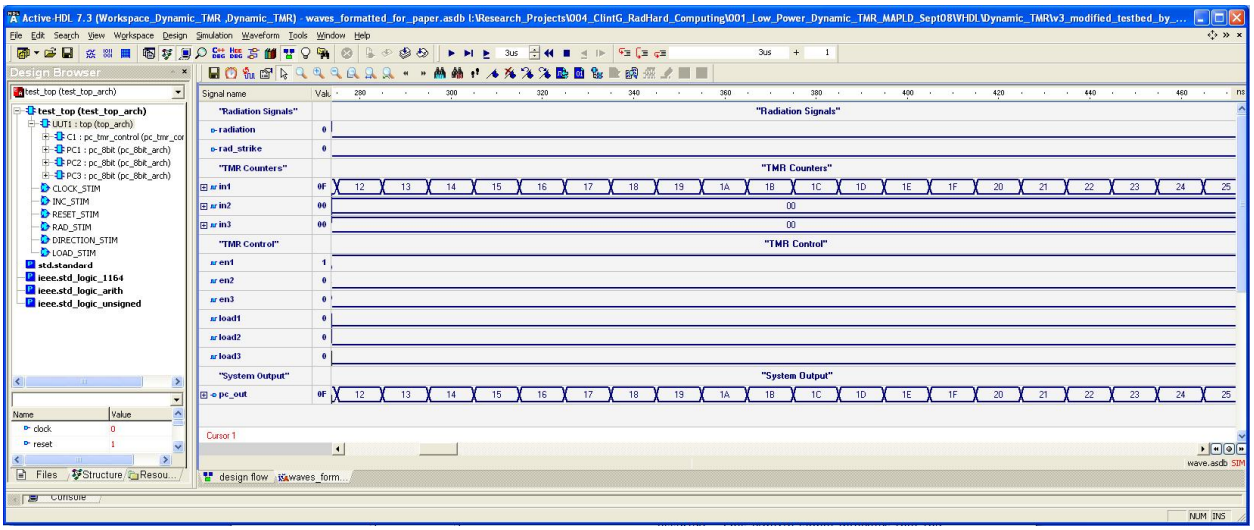

Figure 4. Simulation of Dynamic TMR System When No Radiation is Present

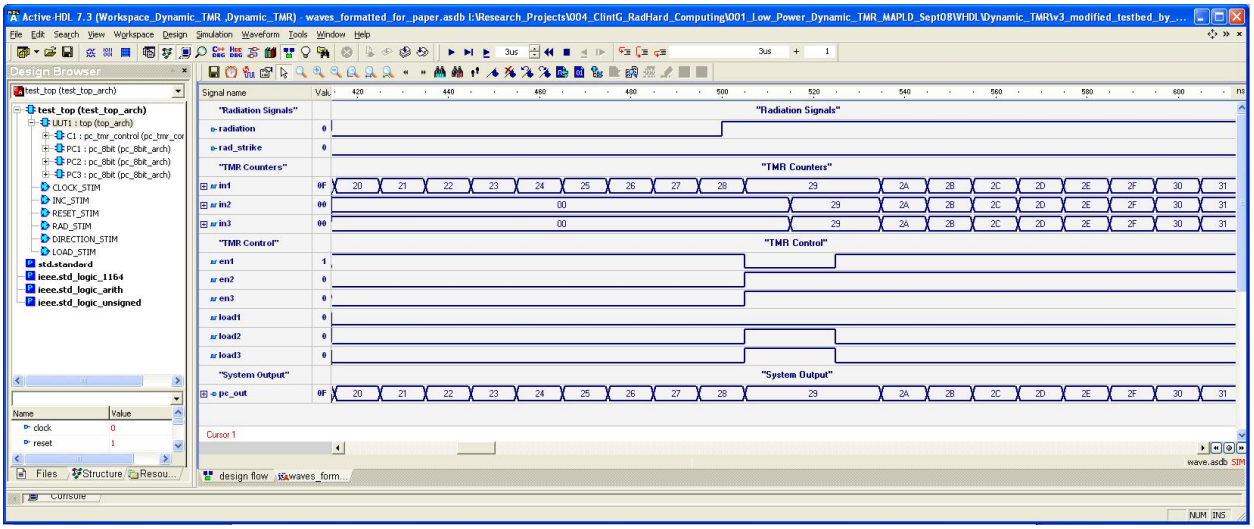

Figure 5. Simulation of Dynamic TMR System When Radiation is Initially Detected

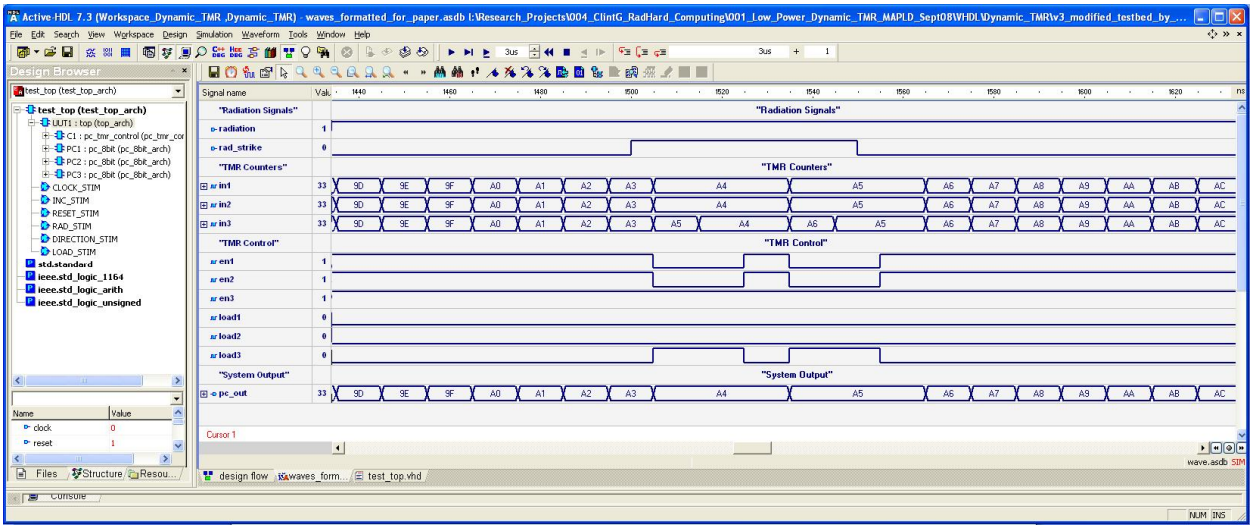

Figure 6. Simulation of Dynamic TMR System Operation in a Heavy Radiation Environment (Including a Correction Example).

FPGA Resources	Resources Used		
	Static TMR	Dynamic TMR	Area Increase
Total # of Slice Registers	39	41	5.1%
# used as Flip Flops	25	27	8.0%
# used as Latches	14	14	0.0%
Total # of 4 Input LUTs	139	143	2.9%
Total Equiv. Gate Count	1291	1319	2.2%

Table 1. Area Usage Comparison Between a Static and Dynamic TMR Approach When Implemented on a Xilinx V-4 FPGA.

V. CONCLUSION

In this paper we presented a dynamic TMR approach to digital computing. This technique is based on an external radiation sensor that indicates when the system is being struck with cosmic particles. In this type of environment, the system uses a traditional TMR approach to fault mitigation. When the sensor indicates that the system is not in a radiation environment, the system disables two of the three redundant counters to reduce power consumption. We applied this approach to a traditional Program Counter and implemented it on a Xilinx Virtex-4 FPGA. We compared the dynamic TMR method to that of a traditional static TMR approach. It was found that the dynamic TMR resulted in an increase of just 2.2% in equivalent gates compared to the traditional static approach yet has the functionality to reach a power savings of up to 66% in low radiation environments.

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